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Intitulé

(Extraction des paramètres électrique d'une diode à barrière de Schottky (SBD) à base de phosphure d'indium de type n (n-InP) par I-V-T et C-V-T)

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Extraction of the electrical parameters of a Schottky barrier diode (SBD) based on n type indium phosphide (n-InP) by I-V-T and C-V-T characteristics

Dissertation in

Micro-Electronics

by

Fritah Abdallah

In Fulfilment of the Requirements for the Degree

of

Doctor of Philosophy

03/07/2017

Dedication

To my dear parents,

who supported me to complete my study and achieve my doctoral degree.

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First of all, I want to thank my supervisor, Pr Lakhdar Dehimi, for taking me on as a student, providing challenging problems to work on and for his guidance, support and patience during this study course. As well as my co-supervisor Dr Saadoune Achour. My research would not have been accomplished without their help.

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ملخص

الوصلة معدن-نصف ناقل تعتبر بنية اساسية في مجال صناعة انصاف النواقل بحكم انها تستخدم في كثير من النبائط المهمة مثل مقحل ماسفات وموسفات لهاذا توصيف السطح بين الناقل ونصف الناقل له أهمية كبيرة. خلال العقدين الأخيرين الخاصيتين سعة-جهد وتيار-جهد هما الأكثر تقنيات التوصيف المستخدمة لدراسة الصمام الثنائي من نوع شوتكي في مجال حرارة واسع.

في هذه الاطروحة بنية شوتكي من نوع Au/n-InP/AuGe تمت دراستها عن طريق الخاصيتين سعة-جهد وتيار جهد في مجال الحرارة 400-100 كلفن وذلك عند تواجد وغياب عيوب السطح و العيوب الداخلية و تيار النفق. هذه المحاكات تمت تنفيذها ببرنامج المحاكات سيلفاكو-تيكاد وذلك بستعمال النماجذ الفزيائية المناسبة لشرح السلوك الغير طبيعي لصمام الثنائي شوتكي الملاحضة تجريبيا وهي انحراف منحنى رتشردسن من الشكل الخطي وأيضا ارتباط عامل المثالية وحاجز شوتكي المستخرج من الخاصية سعة-جهد وتيار-جهد بالحرارة وأخيرا الاختلاف بين حاجز شوتكي المستخرج من الخاصية سعة-جهد وتيار-جهد.

النتائج المتحصل عليها تعطي تفسيرا جديدا لارتباط المعاملات المذكورة سابقا بالحرارة وأيضا الاختلاف بين حاجز شوتكي المستخرج من الخاصية سعة-جهد وتيار-جهد. اضافتا الى ذلك النتائج المتحصل عليها تعطي تفسير محكم لتأثير عدم تجانس حاجز شوتكي وأيضا للنتائج الخاصة بمنحنى رشردسن ومنحنى ريشردسن المعدل باستخدام نموذج ورنر وغتلر وكذلك تأثير العيوب الداخلية على المقاومة التسلسلية وكذلك تقاطع الخاصيات تيار-جهد المقاسة في درجات حرارة مختلفة.

الخاصيتين سعة-جهد وتيار-جهد في مجال حرارة المتحصل عليهما بلمحاكات متوافقة مع المتحصل عليها تجريبيا وذلك بالأخذ بعين الاعتبار عيوب السطح والعيوب الداخلية وتيار النفق.

Abstract

Metal semiconductor (MS) rectifying junction is fundamental structure in semiconductor industry, since it used in important devices such as Metal-semiconductor and Metal-oxide-semiconductor field effect transistors (MESFET and MOSFET), thus the characterization of the MS interface have a great importance. In the last two decades current-voltage (I-V) and capacitance-voltage (C-V) characteristics are most used characterization methods to study Schottky junction in a wade temperature range.

In this thesis, Au/n-InP/AuGe Schottky structure diode was studied by the simulation of I-V and C-V characteristics in the temperature range 400-100 K in absence and presence of interface states, traps and tunneling current. The simulation was performed with Atlas-Silvaco-Tcad device simulator using the appropriate physical models to explain the experimentally observed abnormal behaviors of Schottky diodes which are, the deviation of Richardson plot from linearity, the temperature dependence of the zero-bias barrier height ($\emptyset_{b0}$), capacitance barrier height ($\emptyset_{CV}$) and the ideality factor (n), also the discrepancy obtained between $\emptyset_{b0}$ and $\emptyset_{CV}$.

Our results give new explanation to the temperature dependence of the mentioned parameters and the discrepancy obtained between $\emptyset_{b0}$ and $\emptyset_{CV}$. Moreover the obtained results lead to a coherent explanation of the barrier height inhomogeneity effect, Richardson plot, modified Richardson plot with Werner and Guttler model and modified Richardson plot with Tung model. Also the effect of deep trap on the series resistance and the intersection of I-V curves measured at different temperature were explained.

Good agreement between the simulated I-V-T and C-V-T results and existing experimental data were obtained by considering interface stats, traps and tunneling current.

Résumé

La jonction métal-semiconducteur utiliser comme redresseur est une structure fondamentale dans l'industrie des semiconducteurs, puisqu'elle est utilisée dans des importants dispositifs comme les transistors à effet de champ (MESFET et MOSFET), pour sa la caractérisation de l'interface MS possède une grande importance. Au cours des deux dernières décennies, les caractéristiques courant- tension (I-V) et capacitance-tension (C-V) sont les méthodes de caractérisation les plus utilisées pour étudier la jonction de Schottky dans une plage de température.

Dans cette thèse, la structure de la diode Schottky Au/n-InP/AuGe a été étudié par la simulation des caractéristiques I-V et C-V dans la gamme de température 400-100 K en absence et en présence des états d'interface, pièges et le courant tunnel. La simulation a été effectuée avec le simulateur Atlas-Silvaco-Tcad en utilisant les modèles physiques appropriés pour expliquer les comportements anormaux observés expérimentalement dans les diodes Schottky qui sont la déviation de la courbe linéarité de Richardson, la dépendance de la barrière Schottky ($\emptyset_{b0}$), la barrière extrait à partir de la caractéristique C-V ($\emptyset_{CV}$) et le facteur d'idéalité (n) de la température et aussi l'écart obtenu entre $\emptyset_{b0}$ et $\emptyset_{CV}$.

Nos résultats donnent une nouvelle explication à la dépendance des paramètres mentionnés de la température. En plus, les résultats obtenus conduisent à une explication cohérente de l'effet d'inhomogénéité de la hauteur de barrièr, la courbe de Richardson, et la courbe modifié de Richardson avec le model de Werner et Guttler et la courbe modifié de Richardson avec le model de Tung. En outre notre résultats donne une bonne explication de l'effet des pièges profonds sur la résistance série et l'intersection des courbes I-V mesurées à différentes températures.

Un bon accord à été obtenu entre les caractéristiques I-V-T et C-V-T par simulation et mesurées en prenant en considération les états d'interface, les défauts et le courant tunnel.

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Chapter 1

Schottky barrier diode and InP properties

1.1 Schottky contacts

1.1.1 Schottky barrier formation

The first-order theory of the formation of a Schottky barrier (SB) is the view attributed to Walter Schottky himself originally, and also to Neville Mott in 1939. The Schottky-Mott theory is often violated at a real MS interface since it does not place any emphasis on the MS interface properties. To explain the observed departure of the experimentally obtained SBH from Schottky-Mott relationship, several models was developed based on the concept of Fermi-level pinning (FLP). All this model (gap state models) suggest the presence of an interface specific region (ISR) and surface states in the band gap of the semiconductor named gap states (GS). The gap state models can be divided into two groups, based on whether the metal and the semiconductor are assumed to interact or not [31].

a. Mott-Schottky model

The model proposes that the SBH between a metal and a semiconductor depend only on the work function of the metal $q\Phi_M$ and the electron affinity of the semiconductor $q\chi_S$. as shown in Figure (1.1), the work function is the energy difference between the vacuum level and the Fermi level (the minimum kinetic energy required for an electron to escape from the metal surface in to free space at $T = 0\ K$), where electron affinity is the energy difference between the vacuum and the bottom of the conduction band E_C.

When the metal and the semiconductor are in separate systems the vacuum level is aligned in both materials. After the two materials contacted, electrons flow from the higher to the lower energy level and thermal equilibrium established as a single system. The Fermi levels on both sides will line up leading the creation of a depletion (Schottky case) or accumulation region

(ohmic case) in the semiconductor, depending on the type of the semiconductor and the value of its affinity.

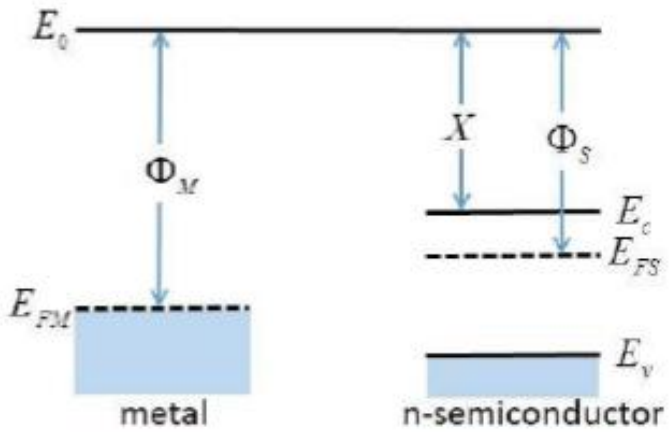


Figure 1.1: Energy band diagram of a Metal and semiconductor before contact.

I. N-type semiconductor with $\Phi_S > \Phi_M$:

After the alignment of the Fermi-levels a depletion layer will created in the semiconductor with the ionized donor N_{d^+} and an accumulation of electrons at the interface of the metal, in which the number of positive charge in the semiconductor is equal to the negative charge at the interface of the metal. The difference between the conduction band and the Fermi-level decrease from the interface to the bulk of the semiconductor, due to the electrical field of the created space charge. The vacuum level moves in the same manner of the conduction band to keep the affinity value constant.

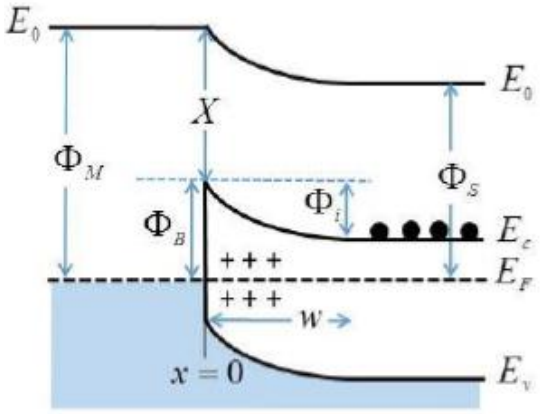


Figure 1.2: Energy band diagram of an ideal Metal-n-type semiconductor in thermal equilibrium.

The energy barrier height at the metal/semiconductor interface shown in Figure 1.2, is the energy needed by electrons to can move from the semiconductor to the metal after thermal equilibrium and is given by:

$$q\,\Phi_{Bn0} = q\left(\Phi_m - \chi_S\right) \tag{1.1}$$

If we apply a positive voltage to the semiconductor with respect to the metal (reverse bias), the semiconductor-to-metal barrier height increases. While Φ_{Bn0} remains constant in this idealized case. If a positive voltage is applied to the metal with respect to the semiconductor (forward bias), the semiconductor-to-metal barrier V_{bi} (built-in voltage) is reduced while Φ_{Bn0} again remains essentially constant. In this situation, electrons can more easily flow from the semiconductor into the metal since the barrier has been reduced.

The energy-band diagrams for the reverse and forward bias are shown in Figure 1.3.

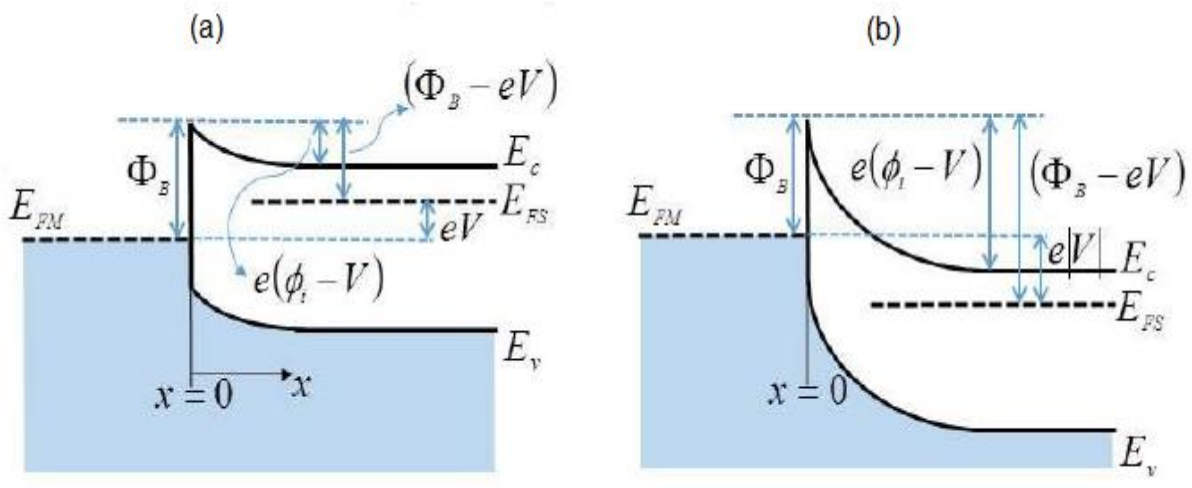


Figure 1.3: Energy band diagram of an ideal Metal-n-type semiconductor: (a), in forward bias (b) in reverse bias.

II. P-type semiconductor with $\Phi_S < \Phi_M$:

After the alignment of the Fermi-levels a depletion layer will created in the semiconductor with the ionized acceptor N_a^- and a deficit of electrons at the interface of the metal. The difference between the conduction band and the Fermi-level increase from the interface to the bulk of the semiconductor, due to the electrical field of the created space charge. The vacuum level moves in the same manner of the conduction band to keep the affinity value constant.

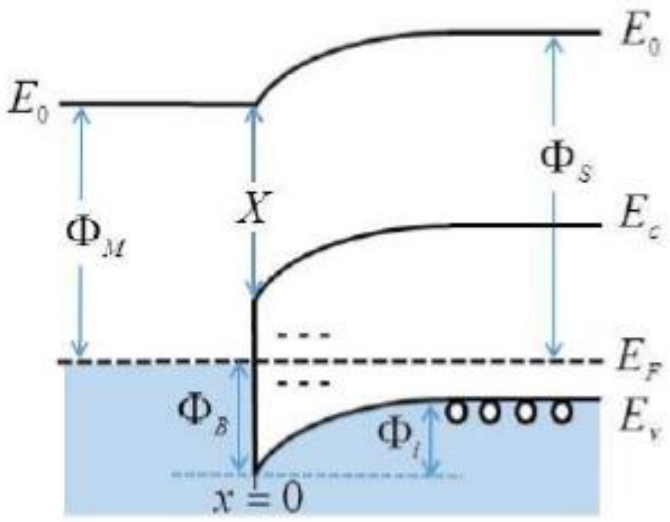


Figure 1.4: Energy band diagram of an ideal Metal-p-type semiconductor in thermal equilibrium.

The energy barrier height at the metal/semiconductor interface (Figure 1.4), is the energy needed to holes can move from the semiconductor to the metal (or equivalently, of electrons from the metal to the semiconductor) after thermal equilibrium and is given by:

$$q\,\Phi_{Bp0} = E_g - q\left(\Phi_m - \chi_S\right) \tag{1.2}$$

Under polarization the behavior of a p-type Schottky diode is the same as n-type Schottky diode, if we replace electrons by holes and Φ_{Bn0} by Φ_{Bp0} [32-34].

b. Fixed-separation models:

The fixed-separation models (separation view of interface states) with the Mott-Schottky model discussed above, comprise the group of non-interacting SBH models. This assumption based on the absence of charge rearrangement at MS interface, in other word it does not give the real overall dipole of the MIS system.

The first model was proposed by Bardeen in 1947 [35] suggesting the surface states localized at the surface of the semiconductor to be the source of the FLP. The barrier in this model depend only to the surface states and is independent to the metal work function. Later in 1965 Cowley and Sze [36] developed a more realistic model, which take into account the effect of both surface states, the metal work function on the SBH and the interface dipole.

Cowley and Sze was derived based on the following assumptions: (1) the contact between the metal and the semiconductor has an interfacial layer of the order of atomic dimensions; it is further assumed that this layer is transparent to electrons with energy greater than the potential barrier but can withstand potential across it. (2) The surface state density (per unit area per

electron volt) at the interface is a property only of the semiconductor surface and is independent of the metal. The schematic shown in Figure 1.5 is the energy band diagram illustrating model.

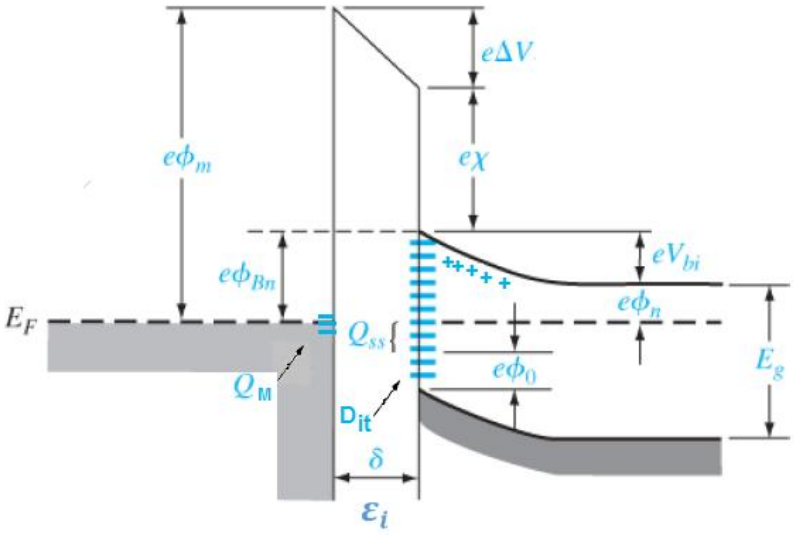


Figure 1.5: Energy band diagram of Metal-n-type semiconductor based on Cowley and Sze model [36].

Where $Ø_m$ is the work function of metal, $Ø_{Bn}$ is the barrier height without image force lowering, $Ø_0$ is the neutral level of interface states, Δ is the potential across interfacial layer, χ is the electron affinity of semiconductor, V_{bi} is the built-in potential, δ is the interfacial layer thickness, ϱ_{sc} space charge density in semiconductor, ϱ_{ss} interface trap charge, ϱ_M surface charge density on metal, D_{it} interface trap density and ε_i is the interface layer permittivity.

With the above assumptions, the barrier height for n-type semiconductor-metal contacts is found to be a linear combination of the metal work function Φ_M and a quantity Φ_0, which is defined as the energy below which the surface states must be filled for charge neutrality at the semiconductor surface. For constant surface state density the theoretical expression obtained is

$$\Phi_{Bn0} = y\left(\Phi_m - \chi_S\right) + (1-y)\left(E_g - \Phi_0\right) - \Delta\,\Phi_{Bn} \tag{1.3}$$

Where y is equivalent to the interface behavior parameter $S = \left(\frac{d\Phi_{Bn0}}{d\Phi_m}\right)$.

$$y = \left(\frac{\varepsilon_i}{\varepsilon_i - q^2\delta D_{it}}\right) \tag{1.4}$$

For a high density of states ($y \ll 1$), the second term on the right hand side of equation (1.3) dominates and the Fermi-level will pinned by interface states close to the level Φ_0. In the case

where interface states are neglected, ($y \simeq 1$) and SBH equation is identical to Mott-Schottky equation (ideal diode).

c. Metal induced gap states model

Metal induced gap states (MIGS) is the first interactive model developed by V. Heine in 1965 [37], he started from assumption that vacuum cleaved surface cannot contain a high density interface states which can pin the Fermi level. The interaction between the metal and semiconductor was expressed by the overlap of wave function at a MS interface, this overlap of wave function alter the electronic structure and the charge distribution in the ISR and induce electronic states in the band gap of the semiconductor.

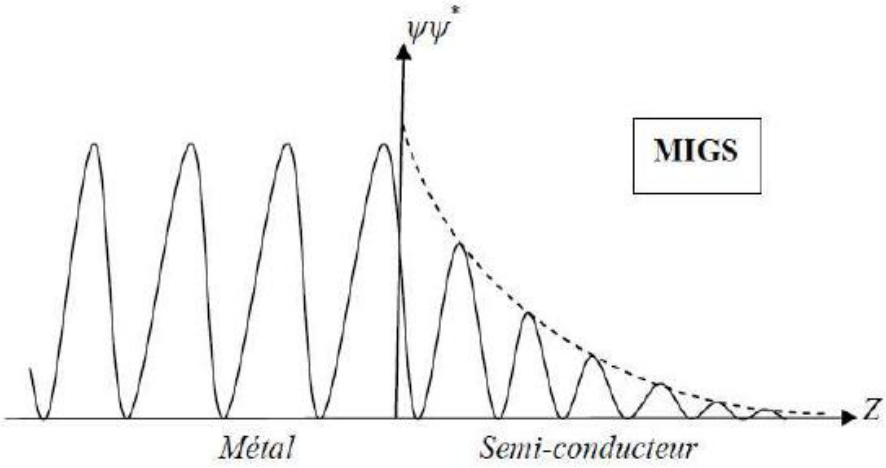


Figure 1.6: Schematic representation of the wave function at metal-semiconductor interface illustrating MIGS concept.

Later in 1977 Louie et al [38] proved the concept theoretically for Al/(Si, GaAS, ZnSe, ZnS) interfaces and gave the MIGS denomination, then the phenomenon has been observed by First et al in 1989 [39] using scanning tunneling microscopy (STM) for Fe/GaAS (110) interface. The band banding is a kind like Figure.1.7.

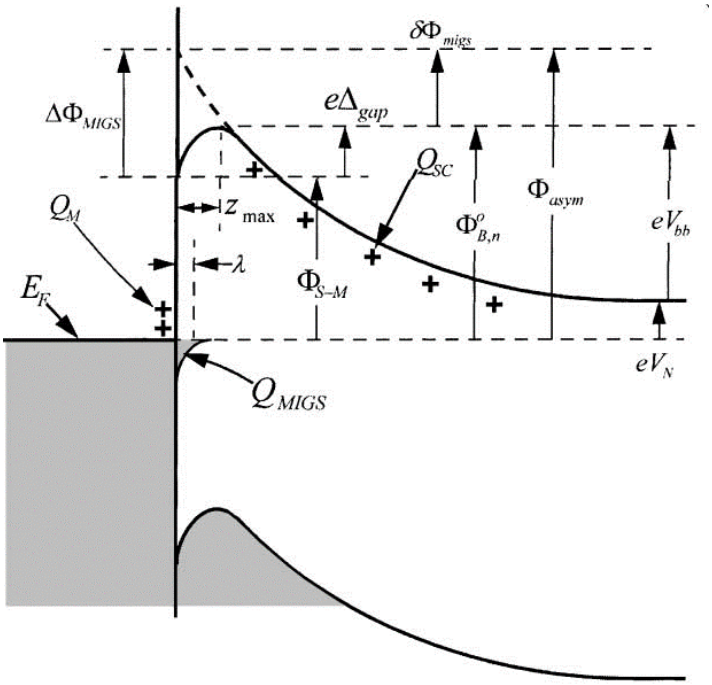


Figure 1.7: Band diagram of the negative charge model, incorporating the effect of the exponential decay of a density of MIGS.

Where Q_{MIGS} is the areal density of the net charge occupied by MGIS, λ is the penetration depth of MIGS into the semiconductor, and $\delta\Phi_{MIGS}$ is the SBH lowering due to MIGS. The effective SBH, which actually controls the electronic transport, is [31]

$$\Phi_{Bn0} = (\Phi_{S-M} + \Delta\Phi_{MIGS}) - \delta\Phi_{MIGS} \tag{1.5}$$

Where

$$\Delta\Phi_{MIGS} \approx -\frac{e\lambda Q_{MIGS}}{\varepsilon_S} \tag{1.6}$$

d. Bond polarization model:

Another interactive approach has been recently developed 2001 by Tung, which is based on the chemical interaction between the metal and semiconductor right at the interface [40]. The model is called Bond polarization theory (BPT). The theory assumes that the charge rearrangement is mostly dependent on the formation of surface bonds, and the Schottky dipole is thought to arise from the polarization of these. In order to calculate this dipole, he applied the electrochemical potential equalization (ECPE) method, which originally is a numerical method for estimating the dipole moment (the measure of the polarity of a chemical bond) of a molecule, and

considered the whole interface to be a gigantic molecule. By using this approach, he was able to calculate the transfer of charge between the atoms, and thus the dipole. The SBH is predicted to be

$$\Phi_B = y_B\left(\Phi_m - \chi_S\right) + (1 - y_B)\frac{E_g}{2} \tag{1.7}$$

$$y_B = 1 - \frac{e^2 d_{MS} N_B}{\varepsilon_{it}(E_g + \kappa)} \tag{1.8}$$

Where y_B is a parameter indicate the interface behaviour, N_B is the density of the chemical bonds, each with a dipole of $e^2 d_{MS}$, d_{MS} is the distance between metal and semiconductor atoms at the interface, ε_{it} is the dielectric screening constant and κ is the sum of all the hopping interactions.

In this model, the ISR was considered as a molecule. A few planes of atoms each from the semiconductor and metal lattices are included in this molecule, consisting a total of N_M metal atoms and N_S semiconductor atoms, each one with the other form the chemical bonds N_B as shown in Figure.1.8 In general, N_B need not equal, and is likely less than the total number of semiconductor (or metal) atoms per unit area of the interface. Lattice mismatch, structure incompatibility, the formation of tilted bonds, etc., all tend to reduce the number of effective bonds formed across an MS interface. Charge transfer is assumed to occur only between atoms directly involved in the interface bonds.

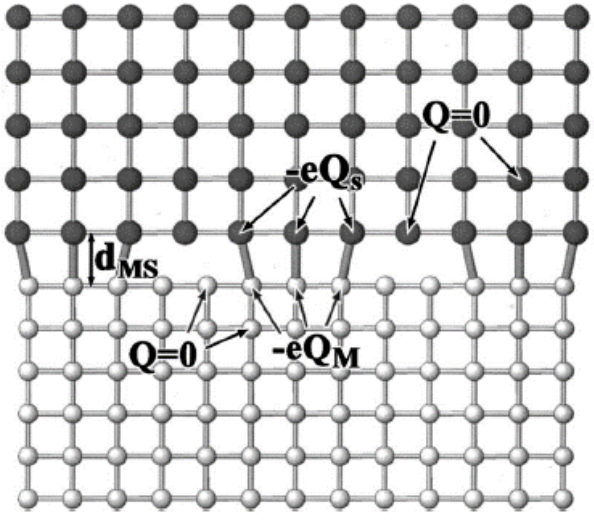


Figure 1.8: A cross-sectional view of the model of a metal semiconductor interface used in the bond polarization theory.

1.1.2. Depletion region

To find the spatial distributions of potential and electric fields, the depletion layer width of a Schottky diode, one needs to solve the Poisson equation in the depletion region using proper boundary conditions. The one-dimensional Poisson equation in the depletion region of a Schottky diode is given by

$$\frac{d^2V(x)}{dx^2} = -\frac{\rho}{\varepsilon_0\varepsilon_s} \tag{1.9}$$

Where ε_0 is the permittivity of free space, and ε_S is the dielectric constant of the semiconductor. The charge density for $0 \leq x \leq W$ is given by

$$\rho = q[N_D - n(x)] \tag{1.10}$$

Where n(x) is the electron density in the space charge region and it is decrease exponentially with distance from the depletion layer edge into the space charge region. Using a one-sided abrupt junction approximation one can obtain the spatial distribution of the electric field by integrating equation (1.9) once, with the result

$$E(x) = -\frac{dV(x)}{dx} = \left(\frac{qN_D}{\varepsilon_0\varepsilon_s}\right)x + C1 \tag{1.11}$$

The constants $C1$ can be determined using the following boundary conditions:

$$E(x) = 0 \quad at \;\; x = W \tag{1.12}$$

By substituting $C1$ into equation (1.11), one obtains the spatial distributions of the electric field inside the depletion region, which is given by:

$$E(x) = \left(\frac{qN_D}{\varepsilon_0\varepsilon_s}\right)(x - W) \tag{1.13}$$

The potential distribution can be obtained by integrating equation (1.13) taking the interface as the potentials origin, which yields

$$V(x) = -\left(\frac{qN_D}{\varepsilon_0\varepsilon_s}\right)\left(\frac{x^2}{2} - Wx\right) \tag{1.14}$$

The depletion layer width W can be expressed in terms of ND, V_{bi}, and Va (applied voltage) across the barrier. From Figure (1.9.a) a and equation (1.14) one obtains the potential at x = W as

$$V(x = W) = V_{bi} - V_a = \frac{qN_D W^2}{\varepsilon_0 \varepsilon_s} \tag{1.15}$$

From eq.2.15, the depletion layer width W is given by

$$W = \sqrt{\frac{2\varepsilon_0 \varepsilon_s (V_{bi} - V_a)}{qN_D}} \tag{1.16}$$

It is seen from equation (1.16) that the depletion layer width is directly proportional to the square root of the applied voltage (*V*a), and is inversely proportional to the square root of the dopant density of the semiconductor. Furthermore, equation (1.16) shows that the depletion layer width decreases with the square root of the forward-bias voltage (i.e., for *V*a ≥ 0), and increases with the square root of the reverse-bias voltage (i.e., for *V*a < 0) [32,41].

The previous approximation is valid for $V_{bi}kT/q \gg 1$. Therefore (2.) is corrected to [42]

$$W = \sqrt{\frac{2\varepsilon_0 \varepsilon_s (V_{bi} - V_a - \frac{kT}{q})}{qN_D}} \tag{1.17}$$

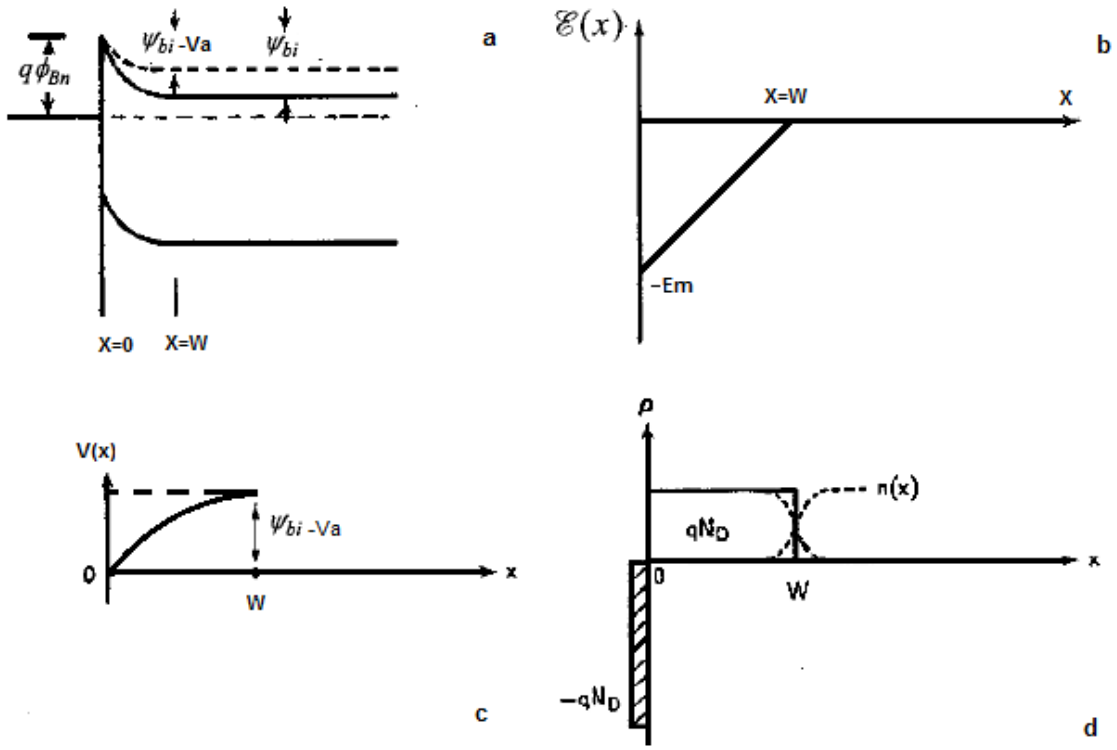


Figure 1.9: (a) Energy band diagram, (b) electric field, (c) potential distribution, and (b) space-charge distribution for a metal/n-type semiconductor Schottky barrier diode.

1.1.3. Capacitance

From Figure (1.9.d) the total space charge Q (per unit area) in the depletion region is

$$Q = qN_D W = \sqrt{2qN_D\varepsilon_0\varepsilon_s(V_{bi} - V_a - \frac{kT}{q})} \tag{1.18}$$

To take into account the charges resulting from the traps in the depletion region, N_D must be replaced by N_{SCR} (ionized impurity in the space charge region). $N_{SCR} = {N_D}^{+} \mp {(n,p)_T}^{-,+}$, where ${n_T}^{-}$ are deep-level or shallow-level acceptors occupied by electrons, and ${P_T}^{+}$ are deep-level or shallow-level donors occupied by holes [43].

The depletion layer capacitance (junction capacitance) per unit area can be obtained by differentiating equation (1.18) with respect to the applied voltage ($C = |dQ/dV|$), which yields

$$C_d = \frac{dQ}{dV_a} = \sqrt{\frac{qN_{SCR}\varepsilon_0\varepsilon_s}{2\left(V_{bi} - V_a - \frac{kT}{q}\right)}} \tag{1.19}$$

Equation (1.19) can also be written as

$$\frac{1}{{C_d}^2} = \frac{2\left(V_{bi} - V_a - \frac{kT}{q}\right)}{qN_{SCR}\varepsilon_0\varepsilon_s} \tag{1.20}$$

By plotting ${1/C_d}^2$ as a function of applied voltage we can find the doping concentration and built-in voltage V_{bi}. If the doping concentration is homogeneous the plot should be linear. $V_{bi} = V' + (kT/q)$, where V' is the extrapolation to the voltage axis such that $1/C_d = 0$. The doping concentration can be determined from the slop via [42]

$$N_{SCR} = \frac{2}{q\varepsilon_0\varepsilon_s}\left[\frac{1}{d\left({C_d}^2\right)/dV}\right] \tag{1.21}$$

1.1.4. Schottky effect

The image-force lowering, also known as the Schottky effect or Schottky-barrier lowering, is the image-force-induced lowering of the barrier energy for charge carrier emission, in the presence of an electric field. When an electric field is applied to the metal surface, electrons

that escape from the metal surface to a distance x in vacuum will create an electric that is same as if an image charge, +q is located at –x from the metal surface (Figure 1.10).

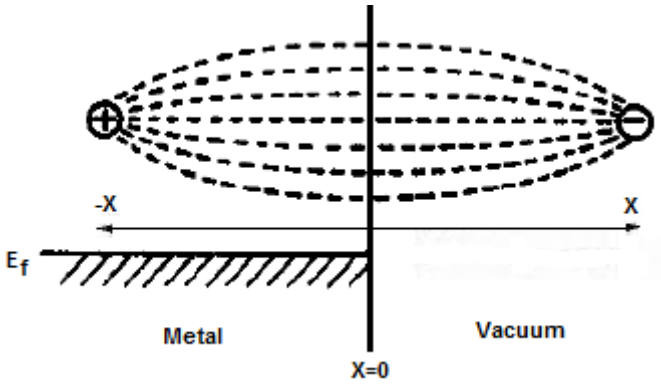


Figure 1.10: The induce image charge inside the metal of Schottky effect.

The positive image charges create a Coulomb attractive force (image force), which tends to pull the escaping electrons back into the metal. The image force can be expressed by

$$F_i = \frac{q^2}{16\pi\varepsilon_0 x^2} \tag{1.22}$$

The potential energy associated with this image force is given by

$$V_i(x) = -\int_{\infty}^{x} F_i dx = -\frac{q^2}{16\pi\varepsilon_0 x^2} \tag{1.23}$$

The potential energy due to the applied electric field can be written as

$$V_a(x) = -qE_x \qquad (\text{for } x \ll W) \tag{1.24}$$

The total potential energy PE as a function of distance is given by the sum

$$V_i(x) + V_a(x) = -\frac{q^2}{16\pi\varepsilon_0 x^2} - qE_x \tag{1.25}$$

The maximum potential energy and the distance where the maximum potential occurs are obtained by differentiating eq.1.25 with respect to *x* and then setting the result equal to 0, which yields

$$x_m = -\frac{q^2}{16\pi\varepsilon_0 E} \tag{1.26}$$

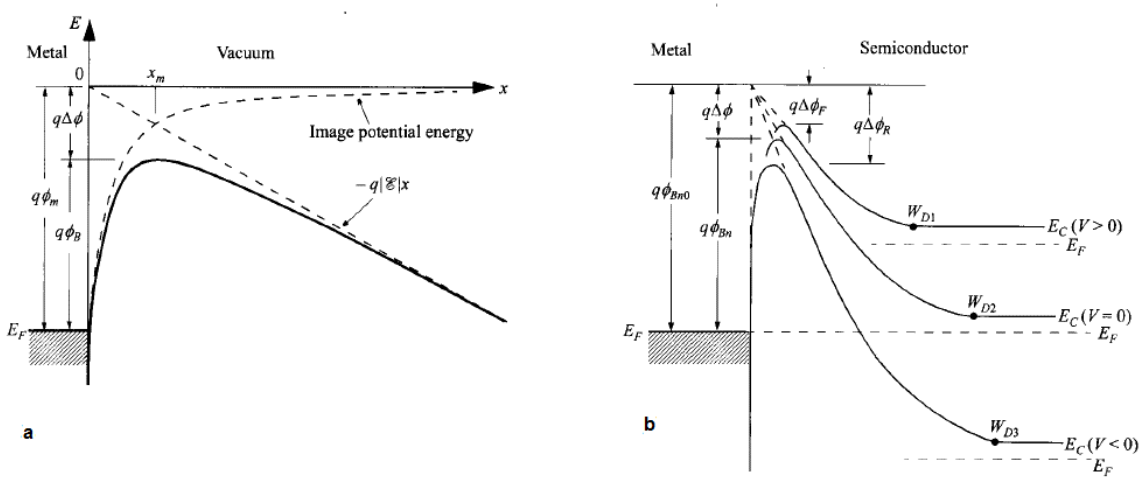


Figure 1.11: Energy band diagram showing Schottky effect at: (a) metal-vacuum interface in the presence of an applied electric field (b) metal-semiconductor interface under different biasing condition.

And

$$V_{m(x_m)} = -q\sqrt{\frac{qE}{4\pi\varepsilon_0}} = -2qEx_m = -q\Delta\emptyset_m \tag{1.27}$$

These results can be applied to metal-semiconductor systems. However, the field should be replaced by the appropriate field at the interface, and the free-space permittivity ε_0 should be replaced by an appropriate permittivity ε_s, characterizing the semiconductor medium, that is,

$$-q\Delta\emptyset = -q\sqrt{\frac{qE_m}{4\pi\varepsilon_s}} \tag{1.28}$$

As shown in Figure (1.11.b) the Schottky effect still occurs even when there is no bias because the electric field is not zero due to the built-in potential. However, the effect of image force lowering is smaller than that in a corresponding metal-vacuum system due to the large values of ε_s [34,41].

1.1.5. Carrier transport mechanisms

The transport through a Schottky junction is dominated by the majority charge carriers, I.e. electrons (holes) in the case of an n-type (p-type) semiconductors, respectively. Figure.1.12 shows the basic transport mechanisms that can contribute to the total current: (1) emission of electrons over the barrier, (2) tunneling through the barrier (3) recombination in the depletion region (4) hole injection from metal. Vérifier

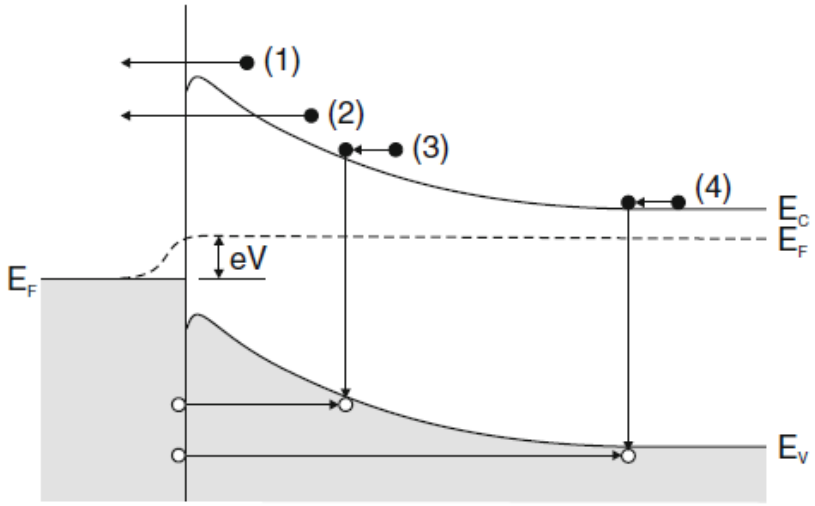


Figure 1.12: The basic transport mechanisms at metal-semiconductor junction.

The transport of electrons above the barrier is the dominant process for ideal Schottky with moderately doped semiconductors operated at moderate or high temperatures. This process was described by three theory, diffusion of Schottky [44], thermionic emission (TE) of Bethe [45] and thermionic emission diffusion (TED) of Sze and Crowell [46]. The current density expressions of the diffusion and thermionic-emission theories, are basically very similar, while TED theory is a combination of the two theories. Here we will discuss thermionic emission theory since it is the most widely used in the interpretation of the experimental I-V characteristics Schottky barrier diodes.

a. Thermionic emission:

The thermionic emission theory is derived by using the assumptions that the barrier height is much larger than kT, so that the Maxwell-Boltzmann approximation applies and that thermal equilibrium is not affected by this process. The current density from the semiconductor to the metal $J_{s\to m}$ is then given by the concentration of electrons with energies sufficient to overcome the potential barrier

$$J_{s\to m} = \int_{E_{Fn}+q\emptyset_{bn}}^{\infty} q v_x dn \qquad (1.29)$$

Where $E_{Fn} + q\emptyset_{bn}$, is the minimum energy required for thermionic emission into the metal, and v_x is the carrier velocity in the direction of transport. The electron density in an incremental energy range is given by

$$dn = N(E)F(E)dE \tag{1.30}$$

Where N(E) and F(E) are the density of states and the distribution function, respectively.

$$dn \approx \frac{4\pi(2m^*)^{3/2}}{h^3}\sqrt{E - E_C}exp\left(-\frac{E - E_C + q\emptyset_{bn}}{kT}\right)dE \tag{1.31}$$

For a given energy *E*, the carrier velocity *v* is determined by

$$E = E_C + \frac{1}{2}m^*v^2 \tag{1.32}$$

Thus, we obtain

$$\sqrt{E - E_C} = v\sqrt{\frac{m^*}{2}} \tag{1.33}$$

And

$$dE = m^*v\,dv \tag{1.34}$$

Therefore, we write equation (1.31)

$$dn \approx 2\left(\frac{m^*}{h}\right)^3 exp\left(-\frac{q\emptyset_{bn}}{kT}\right)exp\left(-\frac{m^*v^2}{2kT}\right)(4\pi v^2 dv) \tag{1.35}$$

Then the one-dimensional integral over $4\pi v^2 dv$ is converted into a three-fold integral over. Integration over all velocities in *y* and *z* directions yields a factor $2\pi\ kT\ /m^*$. The integration over v_x runs from the minimum velocity v_{0x} necessary to pass the barrier

$$\int_{v_{0x}}^{\infty} exp\left(-\frac{m^*{v_x}^2}{2kT}\right)v_x dv_x = \frac{kT}{m^*}exp\left(-\frac{m^*{v_{x0}}^2}{2kT}\right) \tag{1.36}$$

With the minimum velocity determined by

$$\frac{1}{2}m^*{v_{0x}}^2 = q(V_{bi} - V) \tag{1.37}$$

Substituting (2.) into (2.) yields

$$J_{s\to m} = \left(\frac{4\pi q m^* k^2}{h^3}\right) T^2 exp\left(-\frac{q\emptyset_{bn}}{kT}\right) exp\left(\frac{qV}{kT}\right) \quad (1.38)$$

Where $\frac{4\pi q m^* k^2}{h^3}$ called Richardson constant (A^*) and can be rewritten as

$$\frac{4\pi q m_0 k^2}{h^3}\frac{m^*}{m_0} = 120\frac{m^*}{m_0}\ Acm^{-2}k^{-2} \quad (1.39)$$

This current duo to the transport of electrons from semiconductor to metal increase in the forward bias and decrease in the reverse bias duo to the decrease and the increase of the barrier respectively. While the current duo to the transport of electrons from metal to semiconductor $(J_{m\to s})$ does not depend on bias, because the barrier remains constant if we neglect the Schottky effect. Therefore $J_{m\to s}$ can be obtained from the condition $j = J_{s\to m} + J_{m\to s} = 0$ for zero bias. Therefore, the total current density in the thermionic-emission model is

$$J = A^* T^2 exp\left(-\frac{q\emptyset_{bn}}{kT}\right)\left[exp\left(\frac{qV}{kT}\right) - 1\right] \quad (1.40)$$

Where $\left[A^* T^2 exp\left(-\frac{q\emptyset_{bn}}{kT}\right)\right]$ is the saturation current density (j_s).

Multiplying the saturation current density by the surface of the diode (A), the saturation current density j_s and current density J (A/cm^2) becomes the saturation current I_s and the current I (A) respectively.

To take into account the effect of the series resistance (R_S) associated with the bulk material in the semiconductor and the ohmic back contact, and other phenomena that deviate the I-V characteristic from the ideal form such, Schottky effect, equation (1.40) is modified to [47]

$$I = I_s\left[exp\left(\frac{q(V - R_S I)}{nkT}\right) - 1\right] \quad (1.41)$$

Where n is the ideality factor.

b. Tunneling:

Tunneling of electrons thought the barrier potential is an important phenomenon which can dominate the transport process in certain conditions. In contrary of classical physics, the particles in quantum physics can escape the barrier potential even if its energy is below the

maximum of this potential. There is two physical models describing the tunneling phenomenon (Figure 2.13), thermionic field emission (TFE) and field emission (FE).

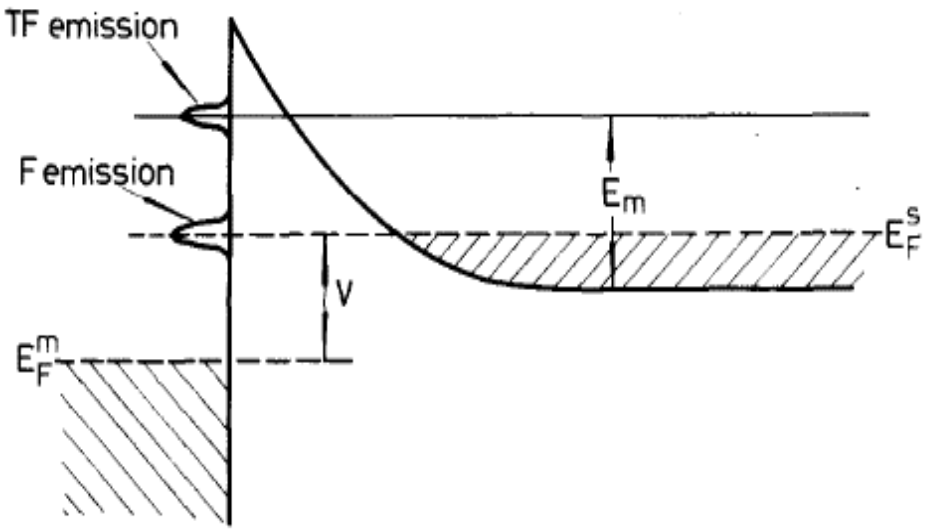


Figure 1.13: Field and thermionic-field emission under forward bias.

Field emission is a pure tunneling process and occur in the case of a degenerate semiconductor at low temperature, where the donor density is so high, and the potential barrier so thin, the current arises from electrons with energies close to the Fermi energy. While thermionic field-emission is tunneling of thermally excited carrier and occur at higher temperature, electrons are excited to higher energies, and the tunneling probability increases very rapidly because the electrons 'see' a thinner and lower barrier. On the other hand, the number of electrons having a particular energy decreases very rapidly with increasing energy, and there will be a maximum contribution to the current from electrons which have an energy above the bottom of the conduction band [48]. According to Padovani and Stratton [49] FE and TEF current can be expressed as

I. forward bias:

$$J = J_s \, exp\left(\frac{E}{E_{00}}\right) \tag{1.42}$$

Where J_s is the saturation current density given by

$$J_{s(FE)} = \frac{2\pi A^* E_{00}\, exp(-E_B/E_{00})}{kT\left[\log\left\{2\left(\frac{E_B - E}{\xi_2}\right)\right\}\right]\sin\left[\frac{\pi kT}{2E_{00}}\log\left\{2\left(\frac{E_B - E}{\xi_2}\right)\right\}\right]} \tag{1.43}$$

$$J_{s(TFE)} = \frac{A^*\left(\pi E_{00}(E_B - E + \xi_2)\right)^{1/2}}{kT\cosh(E_{00}/kT)} exp\left[\frac{\xi_2}{kT} - \frac{E_B + \xi_2}{E_0}\right] \tag{1.44}$$

II. reverse bias:

$$J_{(FE)} = \frac{A^*\pi E_{00} exp\left[-2{E_B}^{3/2}/3E_{00}(E_B - E)^{1/2}\right]}{kT[E_B/(E_B - E)]^{1/2}\sin\left\{\pi kT\frac{[E_B/(E_B - E)]^{1/2}}{E_{00}}\right\}} \tag{1.45}$$

$$J_{(TFE)} = \frac{A^*(\pi E_{00})^{1/2}}{kT}\left[-E + \frac{E_B}{\mathrm{csch}^2(E_{00}/kT)}\right]^{1/2} exp\left(-\frac{E_B}{E_0}\right) \tag{1.46}$$

Where E_B is the potential energy of the top of the barrier with respect to the Fermi level of the metal, E is the potential energy associated with an applied bias V, ξ_2 is the energy of the Fermi level of the semiconductor measured with respect to the bottom of the conduction band, A^* is the effective Richardson constant of the semiconductor and the metal in the case of forward bias and reverse bias respectively, E_0 and E_{00} are the energy given b

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N}{m^*\mathcal{E}_s}} \tag{1.47}$$

$$E_0 = E_{00}\cosh(E_{00}/kT) \tag{1.48}$$

By comparing the thermal energy kT to E_{00} (characteristic tunnelling energy that is related to the tunnel effect transmission probability) one can predict the dominant transport process. When $kT \gg E_{00}$ TE dominates, when $kT \ll E_{00}$ FE dominates and when $kT \approx E_{00}$ TFE is the main mechanism which is a combination of TE and TFE.

1.1.6. barrier inhomogeneities:

Schottky barrier height inhomogeneities can be defined as the lateral variation of the barrier height (along the interface), this lateral variation was attributed to interface propriety and the fabrication process [50-52]. Evidence for the presence of inhomogeneity in the SBH's was

recognized and reported only sporadically before the 1990 [53, 54], the inhomogeneities was described by two parallel diodes with different barrier height and the junction current is a sum of the contribution from the two diodes. These models is in signification error when the SBH varies spatially on a scale less than, or comparable to the width of the space-charge region. The development of the ballistic electron emission microscopy (BEEM) technique [55, 56], provided the spatial resolution needed to examine the distribution of local SBH underneath ultrathin metal layers. Occasionally, large-scale variations (0.7–1.1 eV) of the SBH were observed at compound semiconductor [57]. After 1990 more sophisticated models were developed. Werner and Guttler model [17] and Tung model [16] are discussed next.

a. Werner and Guttler model

The model considered a large area device which contain potential fluctuation or barrier inhomogeneities at the MS interface Figure (1.14) on length a scale, and this potential fluctuation is smaller than the width of the space-charge region, i.e., < 1 μm.

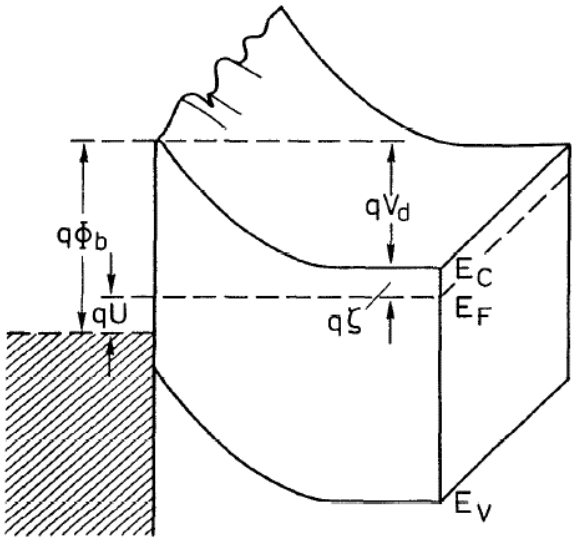


Figure 1.14: Two-dimensional band diagram of an inhomogeneous Schottky contact.

The potential fluctuation was described by a Gaussian distribution of the potential $P\ (V_d)$ with a standard deviation σ_s around a mean $\bar{V}_d$ value according to

$$P(V_d) = \frac{1}{\sigma_s\sqrt{2\pi}} e^{-(\bar{V}_d - V_d)^2/(2{\sigma_s}^2)} \qquad (2.49)$$

By replacing the homogeneous potential in thermionic emission theory with $P\ (V_d)$ and do the integral over the range $[-\infty, +\infty]$ for $J_{s\to m}$ and $J_{m\to s}$, Werner and Guttler found respectively

$$V_d = \bar{V}_d - \frac{q{\sigma_s}^2}{2kT} \tag{1.50}$$

$$\emptyset_{b0} = \bar{\emptyset}_{b0} - \frac{q{\sigma_s}^2}{2kT} \tag{1.51}$$

Than the total current through the inhomogeneous interface is given by

$$I = AA^*T^2 exp\left(-\beta\left(\bar{\emptyset}_{b0} - \frac{q{\sigma_s}^2}{2kT}\right)\right)\left[exp\left(\frac{qV}{kT}\right) - 1\right] \tag{1.52}$$

Where

$$I_s = AA^*T^2 exp\left(-\beta\left(\bar{\emptyset}_{b0} - \frac{q{\sigma_s}^2}{2kT}\right)\right) \tag{1.53}$$

While the capacitance was found to be insensitive to the potential fluctuation that are less than the width of the space charge region, in other words the capacitance depends only on the mean band banding $\bar{V}_d$ and is insensitive to the standard deviation σ_s of the barrier distribution. Thus, ${V^C}_d = \bar{V}_d$ and ${\emptyset^C}_b = \bar{\emptyset}_{b0}$. This result explains the differences of barrier which are derived from capacitance and current.

The authors propose two plots to evaluate the experimental results. The first is the plot of $({\emptyset^C}_b - {\emptyset^j}_b)\ Vs\ T^{-1}$, the plot should yield a straight line. From this plot the standard deviation σ_s can be determined, where the mean barrier $\bar{\emptyset}_b$ is equal to ${\emptyset^C}_b$.

Since the y-axis intercepts of curve (a) and (b) in Figure.1.15 don not exactly equal zero as predicted by Eq.1.51 The authors ascribed this finding to the temperature dependence of σ_s according to

$${\sigma_s}^2(T) = {\sigma_s}^2(T=0) + \alpha_\sigma T \tag{1.54}$$

Where the slope equal to $q{\sigma_s}^2(T=0)/(2k)$ and the y-axis intercept $q\alpha_\sigma/2k$.

Schottky mean barrier itself varies also approximately linearly with T according to

$$\bar{\emptyset}_b(T) = \bar{\emptyset}_b(T=0) + \alpha_{\bar{\emptyset}} T \tag{1.55}$$

Where can $\alpha_{\bar{\emptyset}}$ obtained from the slop of ${\emptyset^C}_b\ Vs\ T$ plot.

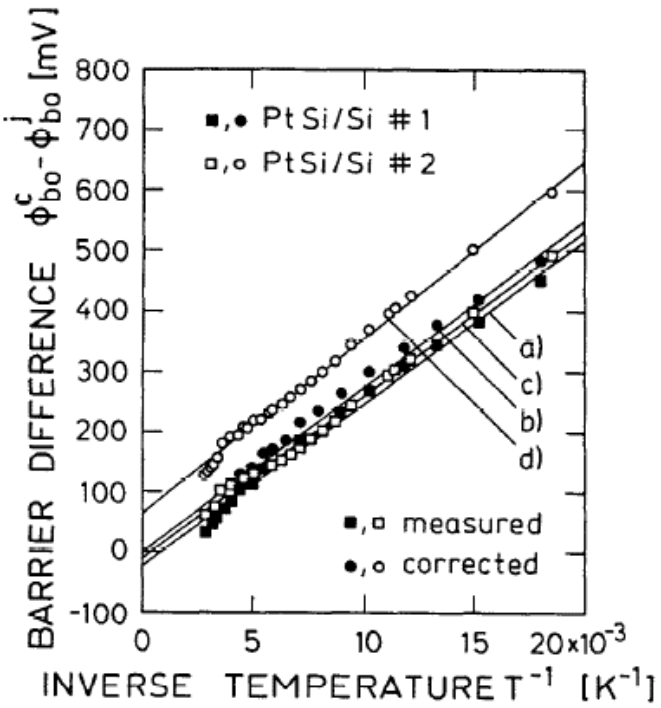


Figure 1.15: Plot of differences between Schottky barriers for two PtSi/Si diodes. Curves (a) and (c) show the difference between values as derived from the conventional evaluation of I/U and C/U data. Curves (b) and (d) follow from curves (a) and (c) after correcting the capacitance barrier for the bias dependence of the mean Schottky barrier according to equation (1.57).

The second is a plot of $(n^{-1}-1)\ Vs\ T^{-1}$. This plot is based on the equation that predicts the temperature dependence of the ideality factor n of inhomogeneous Schottky contacts or so called T_0 problem, the equation is given by

$$n^{-1}-1 = -\rho_2 + \frac{q\rho_3}{2kT} \tag{1.56}$$

Where ρ_2 and ρ_3 are the voltage coefficients $\overline{\emptyset}_b$ (quantify the voltage deformation of the barrier distribution) and can be obtained from the intercept and the slope respectively.
The mean barrier and standard deviation bias dependent are given by [50]

$$\overline{\emptyset}_b - \overline{\emptyset}_{b0} = \rho_2 U \tag{1.57}$$

$$\sigma_s - \sigma_{s0} = \rho_3 U \tag{1.58}$$

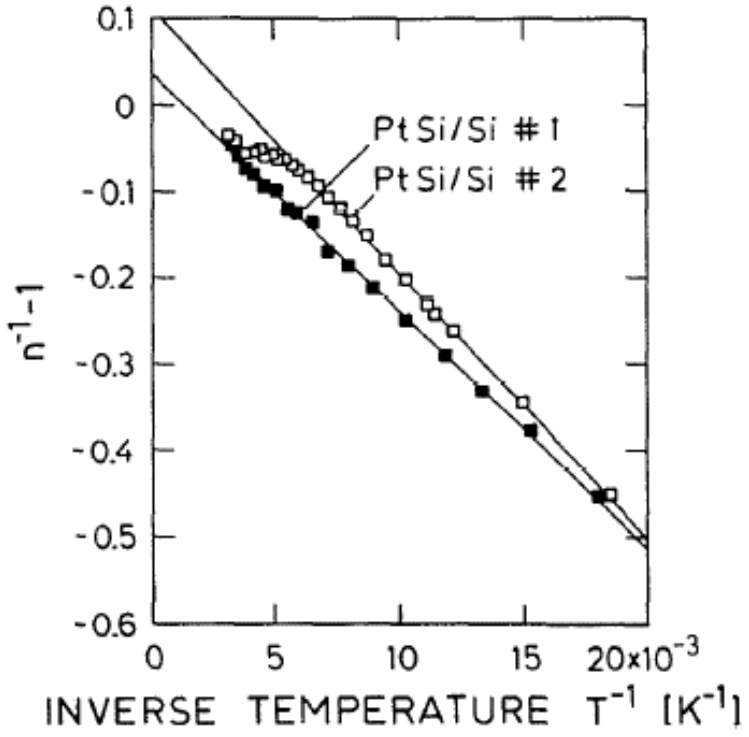


Figure 1.16: The temperature-dependent ideality data of our PtSi/Si diodes follow equation (1.56).

The authors were able to fit several experimental data for Schottky contacts on Si, GaAs, and InP. In addition, the most experiments in the last two decades such as [8, 12, 14, 18, 19], were used this model to interpret the barrier and the ideality factor temperature dependence.
The demerits of this model are absence of interaction between small low barrier regions, the physical reason for the variation of parameters with bias, also the model does not address the length scale of the small low barrier regions [16].

b. Tung model

A cording to Tung [16], the barrier inhomogeneities is a result of the presence of small regions with a low SBH ($\emptyset_{b0} - \Delta$) embedded in an interface with an otherwise uniform high SBH ($\emptyset_{b0}$). Two geometries were considered for the low-SBH region, a small circular patches and narrow semi-infinite strips, as shown schematically in Figure (1.16).

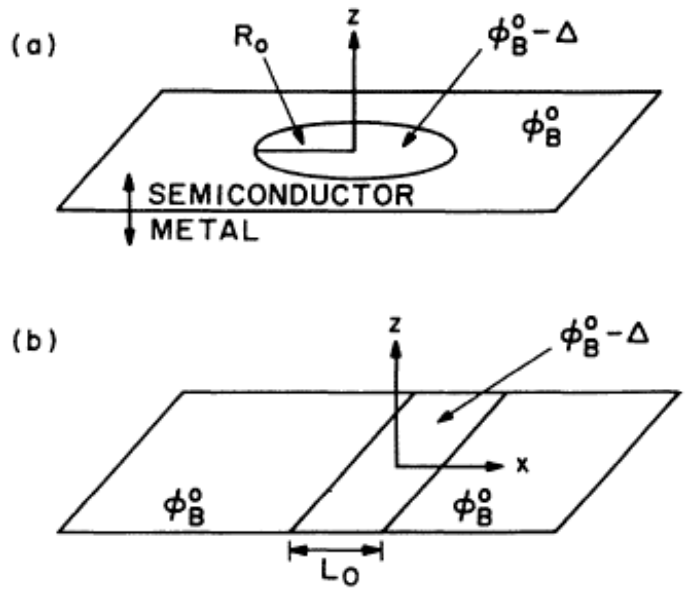


Figure 1.17: Geometries and coordinates of examples of the inhomogeneities in Tung model. (a) Circular patch, (b) narrow strip.

As seen in Figure.1.16, the small regions with low SBH are characterized by two important parameters, the value of the barrier which is lower than the uniform barrier by a value Δ (eV), and the second parameter is the radius R_0 or the length L_0 (for the circular patches and semi-infinite strips respectively) which represent the surface of the small regions with low SBH.
The potential around the circular patch and the narrow strip are given by next equations

$$V(\rho,Z)=V_{bb}\left(1-\frac{z}{W}\right)^2-V_n+V_a-\frac{V_{bb}\Gamma^3 zW^2}{(z^2+\rho^2)^{3/2}} \tag{1.59}$$

$$V(x,y,Z)=V_{bb}\left(1-\frac{z}{W}\right)^2-V_n+V_a-\frac{2V_{bb}\Omega^2 zW}{x^2+z^2} \tag{1.60}$$

Where V_{bb} is the built-in potential of the uniform barrier as function of the applied bias ($V_{bb}=V_{bi}-V_a$), V_n is the difference between the FL and the conduction band maximum (CBM), ρ is the radial coordinate, Γ and Ω are a dimensionless quantity that measures the strength of the patch and the strip respectively.

$$\Gamma^3=\frac{\Delta R_0^2}{2V_{bb}W^2} \tag{1.61}$$

$$\Omega^2=\frac{\Delta L_0}{2\pi V_{bb}W} \tag{1.62}$$

In contrary of the previous model, Tung model take in to account the length scale of the inhomogeneities by introducing the radius R_0 and the length L_0 of the patch and the strip in the potential equation. In addition, it takes in to account the interaction between the small low barriers regions by phenomenon called pinch-off.

A small low barrier region is said to be pinched-off if the carrier need to go over a potential of a neighbour region that has a higher potential. For a large Δ, or smal R_0, the potential in front of the patch is obviously pinched-off. Figure.1.17 illustrates the pinch-off effect by plotting the potential close to a low-SBH patch as a function of the radius R_0, the patch has a $\Delta = 0.2\ (eV)$ and the uniform barrier of the diode $\emptyset_{b0} = 0.8\ (eV)$, which mean that the barrier of the patch equal to $0.6\ (eV)$ $(\emptyset_{b0} - \Delta)$. When the patch's radius has a large value (0.07 um) the potential in close to the patch is equal to the barrier of the patch (0.6 eV), when the patch's radius be smaller the potential in close to the patch reaches a value close to the uniform barrier value (0.8 eV).

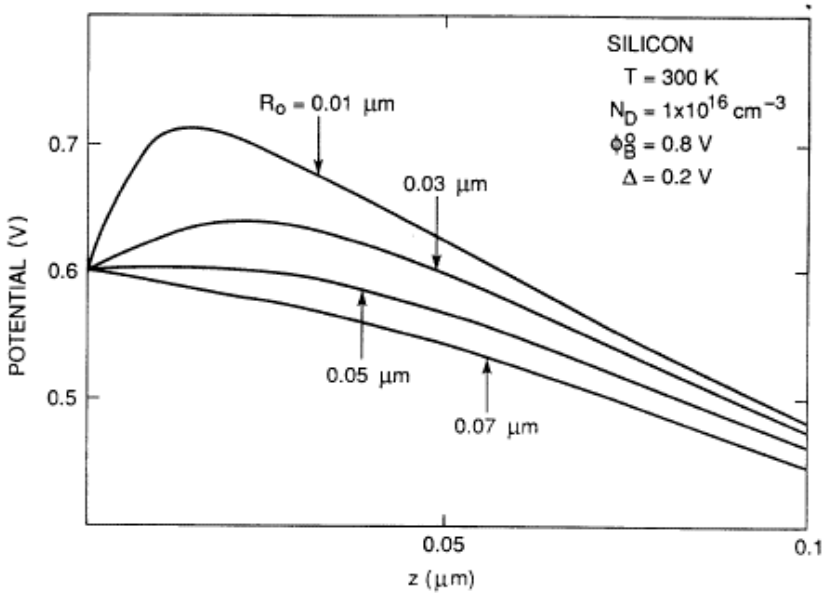


Figure 1.18. CBM potentials along the z axis in close to a low-SBH patch, illustrating the influence of the radius of a low-SBH patch on potential pinch-off.

The condition for pinch-off is obtained from eq.1.59 and eq.1.60 for the patch and the strip respectively

$$\frac{\Delta}{V_{bb}} > \frac{R_0^2}{W} \tag{1.63}$$

$$\frac{\Delta}{V_{bb}} > \frac{\pi L_0}{2W} \tag{1.64}$$

Effectively the total current of inhomogeneous diode is given by two formula depending on the density distribution type of the patches as a function of the parameter γ. Where γ is a constant related to the patch characteristics (a true parameter of the MS interface inhomogeneity) and is given by

$$\gamma = 3\left(\frac{\Delta R_0^2}{4}\right)^{\frac{1}{3}} (cm^{\frac{2}{3}} V^{\frac{1}{3}}) \tag{1.65}$$

The most used expression in the interpretation of experimental results [24-28] is based on one-half of a Gaussian distribution. The density of patches with their parameter γ lying between γ and $\gamma + d\gamma$ is $N(\gamma)d\gamma$:

$$N(\gamma) = \begin{cases} \frac{\sqrt{2}C_1}{\sqrt{\pi}\sigma_1} exp\left(-\frac{\gamma^2}{2\sigma_1^2}\right), & \gamma > 0 \\ 0, & \gamma < 0 \end{cases} \tag{1.66}$$

Where σ_1 $\left(cm^{\frac{2}{3}} V^{\frac{1}{3}}\right)$ is the standard deviation and C_1 (cm^{-2}) is the total density of patches. The strip also has a parameter ω and $N(\omega)$ similar to the parameter γ and $N(\gamma)$ of the patch respectively.

The total current at any given bias is approximately given by

$$\boldsymbol{I_{total}} = A^* A T^2 exp(-\beta \emptyset_{b0})[exp(\beta V_a) - 1]\left[1 + f(V_{bb}) exp\left(\beta^2 \boldsymbol{\kappa} V_{bb}^{\xi}\right)\right] \tag{1.67}$$

Where $\beta = q/kT$, the constants $\boldsymbol{\kappa}$ and $\boldsymbol{\xi}$ and the slowly varying function $\boldsymbol{f}$ are defined in Tab.1.1

Table 1.1: Parameters for electron transport at an inhomogeneous SB with one-half of a Gaussian distribution

Parameter	**Patch**	**Strip**
$\boldsymbol{\xi}$	$\frac{2}{3}$	$\frac{1}{2}$
$\boldsymbol{\kappa}$	$\frac{\sigma_1^2}{2\eta^{2/3}}$	$\frac{\sigma_2^2}{2\eta^{1/2}}$
$\boldsymbol{f(\beta, V_{bb})}$	$\frac{8C_1\sigma_1^2\pi\eta^{1/3}}{9V_{bb}^{1/3}}$	$\frac{C_2\sigma_2^{2/3}\pi\sqrt{\beta}\eta^{1/8}L_{strip}}{1.46V_{bb}^{1/8}}$

Where $\eta = \varepsilon_s/(qN_d)$

The current in equation (1.67) is made up of two components: one being the current over the entire diode, which has a uniform SBH of $\emptyset_{b0}$ and represented by 1 in the last term of equation (1.67), this current dominates at high temperatures and displays near unity ideality factor. The other term represents an additional current due to the presence of the low-SBH patches or strips, at low temperatures this term becomes much larger than 1, and the low-SBH patches dominate at small bias and the ideality factor is larger than 1. In addition, the effect of patches on the I-V characteristic of the diode can be seen clearly, in the reverse bias the current never saturates, while in the forward bias at small values the I-V characteristic shows a curvature or a double diode behaviour Figure (1.19).

One can remark that the parameter γ does not appeared in the total current equation, but is present indirectly by σ_1 which have the same unit.

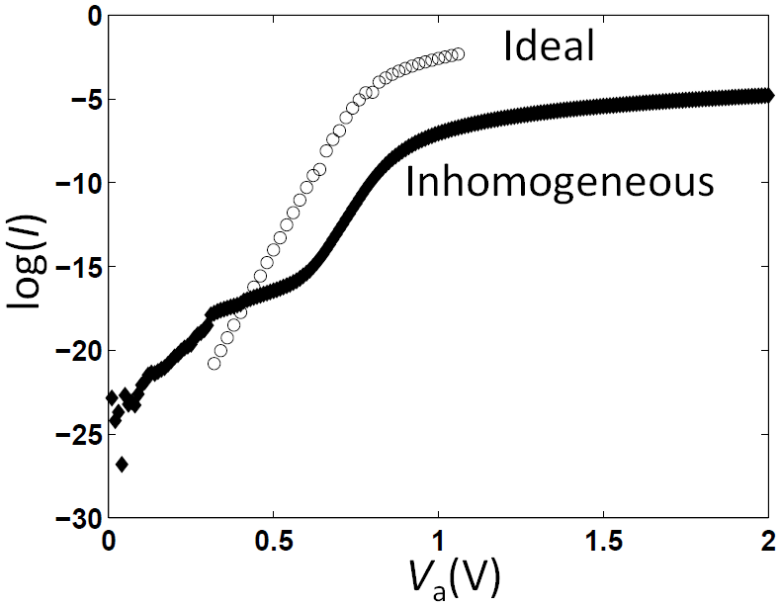


Figure 1.19: Typical current-voltage response of an ideal and inhomogeneous diode [58]

The combined effect of all the low-SBH regions is as if there were a big low-SBH region in the diode with an effective area(A_{eff}) and an effective SBH ($\emptyset_{eff}$).

Even though the effective SBH of each individual patch is roughly temperature independent, but together they may be represented by a temperature dependent effective SBH. That is, at each temperature the current flow through some patches with identical γ. A_{eff} and $\emptyset_{eff}$ of the patches are given by the following relations [25]

$$\emptyset_{eff} = \emptyset_{b0} - \frac{\sigma_1^2}{2kT}\left(\frac{V_{bb}}{\eta}\right)^{\frac{2}{3}} \quad (1.68)$$

$$A_{eff} = A\, C_1 A_p \quad (1.69)$$

Where A_P is the effective area of one patch and is given by

$$A_p = \frac{8\pi\sigma_1^2}{9}\left(\frac{\eta}{V_{bb}}\right)^{1/3} \quad (1.70)$$

From equation (1.68) and equation (1.70) A_P can be rewritten as

$$A_p = \frac{8\pi(2kT)}{9}\left(\frac{\eta}{V_{bb}}\right)(\emptyset_{b0} - \emptyset_{eff}) \quad (1.71)$$

1.2 Material property of indium phusphyde

1.2.1 Cristal structure:

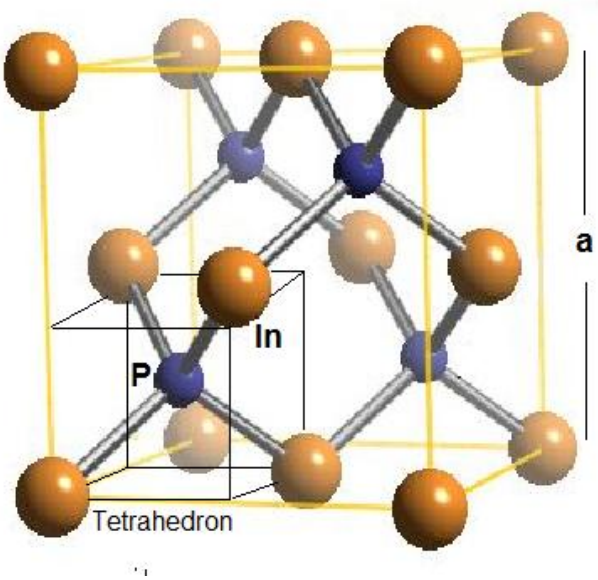


Figure 1.20: Zinc-blende structure for Indium Phosphide

Indium Phosphide (InP) belong to the family of compound semiconductor of III-V groups with Zinc-blende crystal structure like the most III-V group semiconductors, the Zinc-blend structure is similar to the diamond structure except that the two FCC sub-lattices are occupied alternately by two different kinds of atoms (In and P) as shown in Figure.1.20 [41].

1.2.2 Energy band structure:

One of the advantages of InP as III-V group semiconductor over silicon is its direct band gap, which gives strong absorption/emission characteristics that in different optoelectronic devices [1]. The appropriate combination of the band-gap value (1.34 eV at 300 K) and the high atomic numbers Z (49/15) is an advantage of InP over some other compound semiconductors, especially in view of the fabrication of highly efficient photon detectors operating within the temperature range 200–300 K. For example, InP exhibits an absorption efficiency about 3 times higher than GaAs regarding the photons with energy up to 150 keV [59]. The energy band gap structure of InP is shown in Figure (1.21).

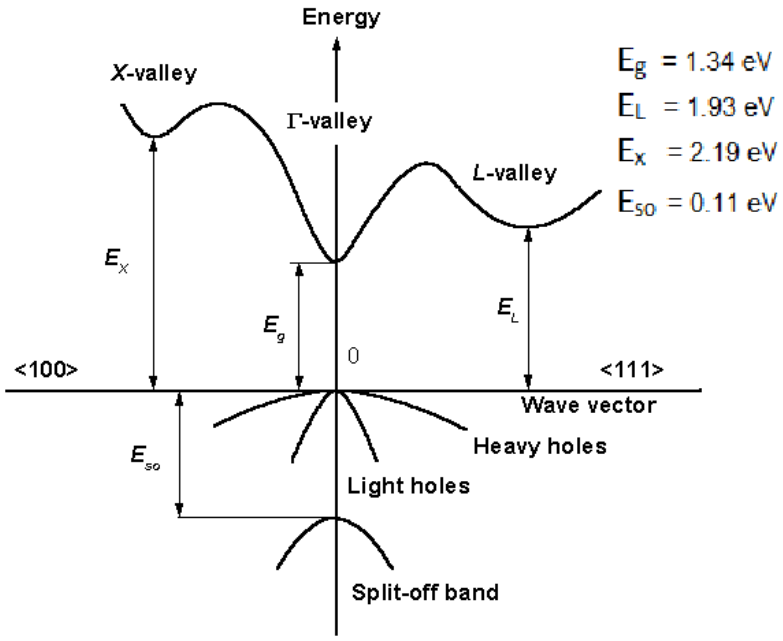


Figure 1.21: Energy band gap structure of InP at 300 K.

1.2.3 Electrical properties:

Concerning the electrical property InP has a very high electron mobility which makes it a particularly attractive material for a steadily increasing number of applications in optoelectronics, high-speed microelectronics and solar-cell devices [2]. Moreover InP offers potentially a fastest operation rate due to its higher electron drift velocity in the electric field region (about 10^4 V/cm) mostly used for detector operation, and this value increases at low temperature and is higher by several times than is offered by GaAs working in the saturation drift velocity regime [59]. Furthermore, InP is more radiation resistant than Si and GaAs, this

is a very important advantage not only to space solar cells but also to the electrical property, because the radiation can affect the mobility and the carrier diffusion length [4, 60]. Table (1.2) shows several important parameters used in the simulation.

Table 1.2: Important parameters of InP at 300 K

Parameter		Value	Unit
Effective mass	Electron m_n/m_0	0.08 [63]	
	Hole m_p/m_0	0.69 [63]	
Richardson constant	N-type	9.6 [63]	A K^{-2} cm^{-2}
	P-type	82.8 [63]	
Affinity		4.38 [63]	eV
Dielectric constant $\varepsilon_s/\varepsilon_0$		12.5 [63]	
Effective density of stats	CB	$5.7\ 10^{17}$ [61]	cm^{-3}
	VB	$1.1\ 10^{19}$ [61]	
Thermal velocity	Electron	$3.9\ 10^{5}$ [61]	m s^{-1}
	Hole	$1.7\ 10^{5}$ [61]	
Auger coefficient	Electron	$3.7\ 10^{-31}$ [61]	Cm^6 s^{-1}
	Hole	$8.8\ 10^{-30}$ [61]	

1.2.4 Doping:

The doping of InP can be done by various material from the second, fourth and sixth group of the periodic table. A n-InP can be obtained if the Indium atoms in the Indium sublattices are replaced by Si, Sn and Ge element of the group-IV, or if the phosphor atoms in the Phosphor sublattices are replaced by S element of the group-VI. A p-InP can be obtained if the phosphor atoms in the Phosphor sublattices are replaced by a group-IV element or if the Indium sublattices are replaced by a group-II element, Zn and Be are widely used [41]. The ionization energy of the mentioned shallow donor is 0.0057 eV, while ionization energy of the shallow acceptor are 0.035 eV for Zn and 0.03 eV for Be [61]. Using solid-source molecular beam epitaxy (SSMBE) 1.1×10^{20} Perhaps is the highest doping concentration level ever reported for Si-doped InP layers [62].

1.2.5 Interface:

In the laboratory environment, a chemically cleaned semiconductor crystal surface is usually covered with layers of native oxides even when it is exposed to clean room air for a very short time, in addition if the semiconductor surfaces are prepared by the usual polishing and chemical etching, and the evaporation of metal is carried out in a conventional vacuum system having a pressure of around 10^{-5} torr, their surfaces are inevitably covered with an undesirable native oxide film [7,8,10].

For InP semiconductor the chemical composition of native oxides that can be grown on its surface are $InPO_4$, $In(PO_3)_3$, P_2O_5 [5,7,8,11].

Chapter 2

Physical models and simulation software

2.1 Physical model used in simulation:

Here we describe the physical models used in the simulation of the present work, the simulation software Atlas-Silvaco-Tcad and the statements that activate these physical models and Atlas-Silvaco TCAD.

2.1.1 Density of stats:

The temperature dependence of the density of states is given with the Next relation

$$N_{c,v} = \left(\frac{T}{300}\right)^{Nc,v.F} \times N_{c,v}(300\ K) \qquad (2.1)$$

Where $Nc.F$ and $Nv.F$ are material parameters and are equal to 1.5 [61, 64].

2.1.2 Bang gap:

The temperature dependence of the band gap energy is modeled with Varshni's empirical relationship [65]

$$\mathrm{E_g(T)} = \mathrm{E_g(0)} - \frac{\alpha \mathrm{T}^2}{\mathrm{T}+\beta} \qquad (2.2)$$

Where, T is the lattice temperature, $E_g(0)$=1.42 (eV) is the band gap at 0 K, $\alpha = 4.9 \times 10^4$ (eVK^{-1}) and β=327 K are material parameters [66]

2.1.3 Low field mobility:

Since there is no need to the doping concentration dependent according to the diode structure, we used a constant low-field mobility model that does account just for lattice scattering due to temperature [61]

$$\mu_{n,p} = \mu_{n0,}\mu_{p0,}\left(\frac{T}{300}\right)^{-\gamma_n,\gamma_p} \tag{2.3}$$

Where, T is the lattice temperature, $\mu_{n0,} = 4300$ $\mu_{p0,} = 173$ $cm^2V^{-1}s^{-1}$ are respectively the electron and hole mobility in 300 K of n-InP with 1.2E16 cm^{-3} doping concentration [67], γ_n, γ_p are material parameters [61]

2.1.4 Shockley-Read-Hall:

To take into account the effect of the traps used in the simulation on the recombination of the electrons, the standard SRH recombination term is modified as follows [64].

$$R = \sum_{\beta=1}^{m} R_{A_\beta} \tag{2.4}$$

Where m is the number of acceptor-like traps, the function R given as flow

$$R_{A\beta} = \frac{pn - n_{ie}^2}{\tau_n\left[p + \frac{1}{g} + n_{ie}\exp\left(\frac{E_i - E_t}{kT_L}\right)\right] + \tau_p\left[n + g + n_{ie}\exp\left(\frac{E_t - E_i}{kT_L}\right)\right]} \tag{2.5}$$

The electron and hole lifetimes τ_n and τ_p are related to the carrier capture cross sections σ_n and σ_p through the Equations:

$$\tau_{n,p} = \frac{1}{\sigma_{n,p}\, v_{n,p}\, N_T} \tag{2.6}$$

v_n, v_p are the thermal velocities for electron and hole respectively.

2.1.5 Auger recombination:

Auger Recombination is commonly modeled using the expression [68]

$$R_{Auger} = C_n(pn^2 - nn_{ie}^2) + C_p(np^2 - pn_{ie}^2) \tag{2.7}$$

Where C_n, C_p are the auger coefficient for electron and hole of the InP semiconductor respectively [69].

2.1.6 Impact ionization:

Zappa developed a model for temperature and field dependent ionization rates in InP semiconductor [70]

$$\alpha,\beta(\mathrm{E},\mathrm{T}) = \frac{\mathrm{qE}}{\mathrm{E}_{\mathrm{th}}^{\alpha,\beta}} \exp\left\{ 0.217\left(\frac{\mathrm{E}_{\mathrm{th}}^{\alpha,\beta}}{\mathrm{E}_{\mathrm{R}}^{\alpha,\beta}}\right)^{1.14} - \left[\left(0.217\left(\frac{\mathrm{E}_{\mathrm{th}}^{\alpha,\beta}}{\mathrm{E}_{\mathrm{R}}^{\alpha,\beta}}\right)^{1.14}\right)^2 + \left(\frac{\mathrm{E}_{\mathrm{th}}^{\alpha,\beta}}{\mathrm{qE}\lambda^{\alpha,\beta}}\right)^2\right]^{0.5}\right\} \quad (2.8)$$

Where $\lambda^{\beta}, \lambda^{\alpha}, E_R^{\alpha}, E_R^{\alpha}, E_{th}^{\alpha}, E_{th}^{\alpha}$ are material parameters [33], T is the local temperature and E is the local electric field.

2.1.7 Incomplete ionization of impurities:

The dependence of ionized donor (N_D^+) on temperature is modeled using Fermi-Dirac statistics with the appropriate factor for conduction-band and with the introduction of quasi-Fermi level for electron [71] as

$$N_D^+ = \frac{\mathrm{N_D}}{1 + 2\exp\left(\frac{\mathrm{E_{F_n}} - \mathrm{E_D}}{\mathrm{kT_L}}\right)} \quad (2.9)$$

Where N_D is the n-type doping concentration, E_{F_n} is the electron quasi-Fermi level, E_D is the donor impurity level.

2.1.8 Thermionic emission:

We can describe thermionic emission current flow in terms of an effective recombination velocity at the surface of the semiconductor.

$$J = q(n_m - n_0)v_R \quad (2.10)$$

$$v_R = \frac{\mathrm{A^*T^2}}{\mathrm{qN_c}} \quad (2.11)$$

Where n_m is the electron density at x_m when the current is flowing, n_0 is quasi equilibrium electron density at x_m

$$n_0 = N_c \exp(-q\psi_B/k\mathrm{T}) \quad (2.12)$$

$$n_m = N_c \exp\{q[\varphi(x_m) - \psi_B]/\mathrm{kT}\} \tag{2.13}$$

ψ_B is the Schottky barrier at the MS interface, $\varphi(x_m)$ is the applied voltage at x_m.

2.1.9 Universal Schottky tunneling:

The key feature of the model is that tunneling current through the barrier is converted into a local generation or recombination process where the local rate, $G_{Tun}(r)$ depend on the local Fermi-level, ϕ_n and the potential profile along the tunneling path [72].

$$\mathrm{G_{Tun}(r)} = \frac{\mathrm{A^*T}}{\mathrm{k_B}} \vec{\mathrm{E}}\, \Gamma(\mathrm{r}) \ln\left[\frac{1 + \exp(-\mathrm{q}(\psi - \phi_\mathrm{n})/\mathrm{k_B T})}{1 + \exp(-\mathrm{q}(\psi - \phi_\mathrm{m})/\mathrm{k_B T})}\right] \tag{2.14}$$

Where J_{Tun} is the total tunneling current density, A^* is the Richardson constant, T is the lattice temperature, $E_{Fm} = -q\phi_m$is the Fermi-level for the metal, $E_{Fn} = -q\phi_n$ is the electron Quasi Fermi-level in the semiconductor, and $\Gamma(r)$is the tunneling probability.

$$\Gamma(r) = \exp\left[-\frac{2}{\hbar}\int_0^r \sqrt{2m\left(\phi_b/q + \emptyset_m - \psi(x)\right)}dx\right] \tag{2.15}$$

2.1.10 Image force lowering:

The image-force lowering, also known as the Schottky effect or Schottky-barrier lowering, is the image-force-induced lowering of the barrier energy for charge carrier emission, in the presence of an electric field.

$$\Delta\emptyset = \sqrt{\frac{qE_m}{4\pi\varepsilon_s}} \tag{2.16}$$

Where, ε_s and E_m are the semiconductor permittivity and the electrical field at the interface.

2.2 The simulation software:

The simulation was performed with Atlas-Silvaco-Tcad provides a general capabilities for physically-based two and three-dimensional simulation of electrical, optical, and thermal behavior of semiconductor devices.

The device structure can be defined by specifying the regions, materials, doping profile and doping concentration onto a two or three dimensional with specified mesh. The mesh is defined by a series of horizontal and vertical lines and the spacing between them, the intercept between this lines called nodes.

The electrical characteristics of the device can be achieved by solving the continuity equations, Poisson equation and the transport equations with specified numerical method in each node in specified bias conditions using the materials parameters of each region.

Poisson equation including the carrier concentrations, the ionized donor and acceptor concentrations calculated by the incomplete ionization model, charge due to traps and defects. Fermi-Dirac statistics and the density of states are used to calculate the electron and the hole concentrations and the quasi-Fermi levels. The generation and recombination rates in the continuity equations including the generation and recombination rates calculated by the generation and recombination models.

For the bias conditions, the DC solution was used to calculate the IV characteristics and the AC small signal solution to calculate the CV characteristics.

In the next sections will discover how a code can be defined in atlas of Silvaco-Tcad software and the statements that activate the previous physical models.

2.2.1 Atlas inputs and outputs:

Figure (2.1) shows the types of information that flow in and out of Atlas. Most Atlas simulations use two input files. The first input file is a text file that contains commands for Atlas to execute. The second input file is a structure file that defines the structure that will be simulated.
Atlas produces three types of output files. The first type of output file is the run-time output, which gives you the progress and the error and warning messages as the simulation proceeds. The second type of output file is the log file, which stores all terminal voltages and currents from the device analysis. The third type of output file is the solution file, which stores 2D and 3D data relating to the values of solution variables within the device at a given bias point.

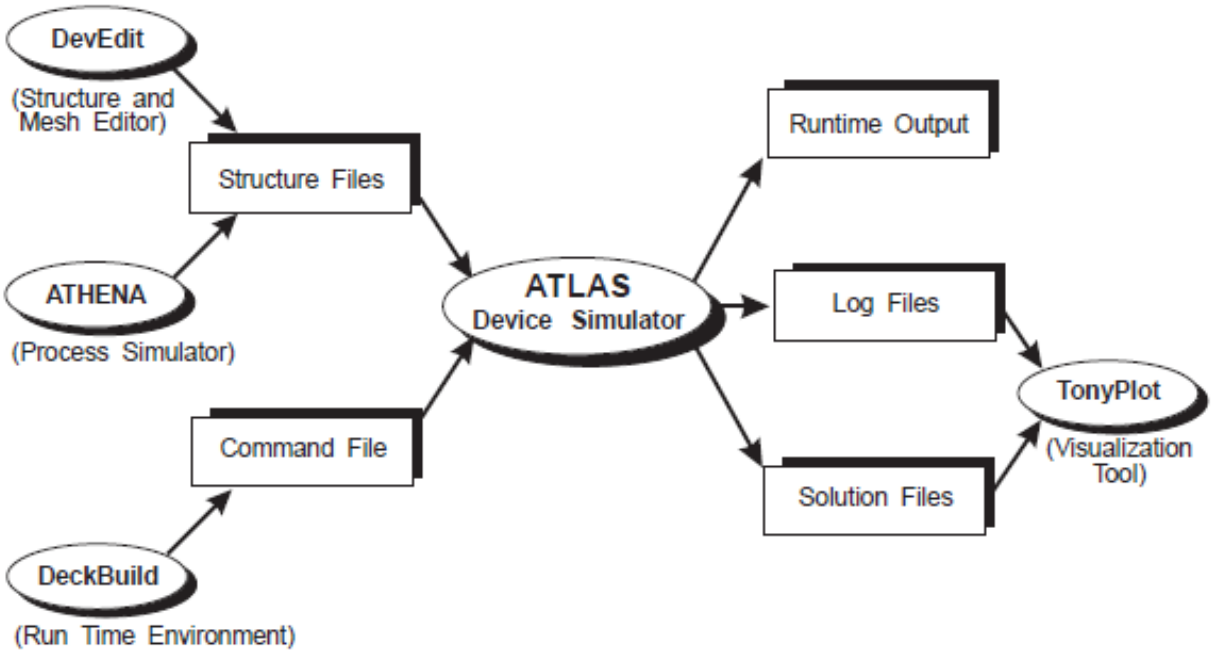


Figure 2.1: Atlas inputs and outputs

The used input in this work is command file or the code in the Deckbuild (an interface between the user and Atlas simulator which contain two windows, one for the input command file and the second for the output run time file). To run Atlas inside Deckbuild the code must started with the statement GO ATLAS, also a single input file may contain several Atlas runs each separated with a go atlas line.

2.2.2 The Atlas commands:

Atlas commands consist of a sequence of statements. Each statement consists of a keyword that identifies the statement and a set of parameters. The general format is:
<STATMENTS> <PARAMETER > = <VALUE>

For any <STATEMENT>, Atlas may have four different types for the <VALUE> parameter. These are: Real, Integer, Character, and Logical.

Atlas can read up to 256 characters on one line. But it is better to spread long input statements over several lines to make the input file more readable. The \ character at the end of a line indicates continuation.

An Atlas code must has five groups of statements that must occur in the order illustrated in Figure (2.2).

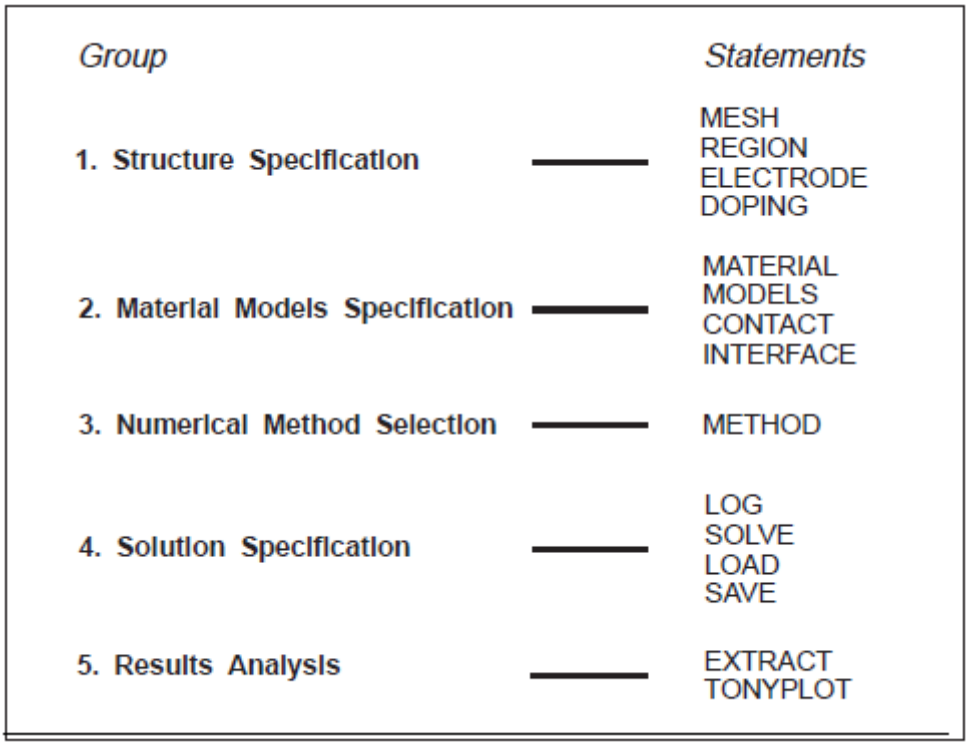


Figure 2.2: Atlas command with the primary statements in each group.

a. Structure specification:

There are three ways to define a device structure in Atlas.

The first way is to read an existing structure from a file. The structure is created either by an earlier Atlas run or another program such as Athena or DevEdit. A MESH statement loads in the mesh, geometry, electrode positions, and doping of the structure. For example:

MESH INFILE=<filename>

The second way is to use the Automatic Interface feature from DeckBuild to transfer the input structure from Athena or DevEdit.

The third way is create a structure by using the Atlas command language, which is the way used in our code. In this case the information described in the following four sub-sections must be specified in the order listed.

I. Specifying the initial mesh:

The first statement in structure declaration is the mesh statement. Mesh statement allows the user to specify many structure type, rectangular, circular and cylindrical each of these structure type can be defined in 2 or 3 dimension. Here will see how to define a 2D cylindrical structure.

The first statement must be:

MESH CYLINDRICAL

This is followed by a series of X.MESH and Y.MESH statements.

X.MESH LOCATION=<VALUE> SPACING=<VALUE>

Y.MESH LOCATION=<VALUE> SPACING=<VALUE>

The X.MESH and Y.MESH statements are used to specify the locations in microns of vertical and horizontal lines, respectively, together with the vertical or horizontal spacing associated with that line. The X.MESH and Y.MESH statements must be listed in the order of increasing x and y. Both negative and positive values of x and y are allowed. Atlas sets some limits on the maximum number of grid nodes that can be used. In the default version, 2D Atlas simulations have a maximum node limit of 100,000.

In cylindrical coordination Atlas operates with x=0 as the axis of symmetry around which the cylindrical geometry is placed. The calculated current is in Amps rather than the usual Amps per micron.

The CYLINDRICAL parameter setting isn't stored in mesh files. Therefore, this parameter must be specified each time a mesh file, which contains cylindrical symmetry, is loaded

MESH INF=NAME.STR CYLINDRICAL

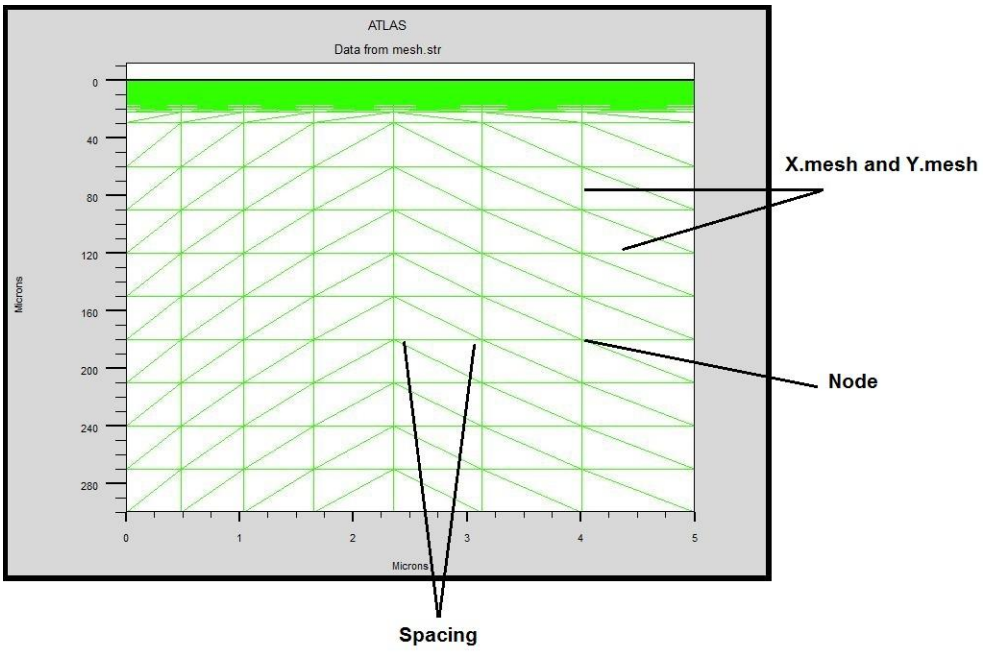


Figure.2.3: Meshing example in atlas.

Specifying a good grid is a crucial issue in device simulation but there is a trade-off between the requirements of accuracy and numerical efficiency. Accuracy requires a fine grid that resolves the structure in solutions. Numerical efficiency is greater when fewer grid points are used. The critical areas to resolve are difficult to generalize because they depend on the technology and the transport phenomena. For Schottky barrier diode the critical area is in the interface between metal and semiconductor.

The CPU time required to obtain a solution is typically proportional to N^{α}, where N is the number of nodes and α varies from 2 to 3 depending on the complexity of the problem. Thus, the most efficient way is to allocate a fine grid only in critical areas and a coarser grid elsewhere. The three most important factors to look for in any grid are:

- Ensure adequate mesh density in high field areas.
- Avoid abrupt discontinuities in mesh density.

II. Region:

Region statements specifies the location of materials in a previously defined mesh. The region numbers must start at 1 and are increased for each subsequent region statement. In Atlas the maximum regions that can be defined is 15000. The region statement is given as flow

REGION NUMBER=<INTEGER> MATERIAL= <CHARACTER> <POSITION PARAMETERS>

The position parameters are specified in microns using the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters.

III. Electrode:

Once the regions and materials are specified, at least one electrode that contacts a semiconductor material must defined. This is done with the ELECTRODE statement. For example:

ELECTRODE NAME=<ELECTRODE NAME> <POSITION_PARAMETERS>

You can specify up to 50 electrodes. The position parameters are specified in microns using the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters.

IV. Doping:

The doping profiles can be specifies either analytically or from an input file. The doping statement must contain the distribution type of doping, the doping concentration, the dopant type and the position parameters. The position parameters can be define by x.min, x.max, y.min and y.max or by material type or by region number. For example can be specify as flows

DOPING N.TYPE CONC=1.2E16 UNIFORM MATERIAL=INP

b. Material and model specification:

After the definition of the structure the material parameters, physical model, the contact and interface specification must be given in this sequence to Atlas used during the device simulation. Most the physical model are defined in the model statement except some physical model such impact ionization which is enabled in impact statement.

I. Specifying material properties:

All materials are split into three classes: semiconductors, insulators and conductors. Each class requires a different set of parameters to be specified. For semiconductors, these properties include a lot of parameters such as electron affinity, band gap, density of states …, There are default parameters for material properties used in device simulation for many materials but is better to define the parameters manually. If a material does not exist then it must defined with the name of existing material using its own parameters values instead the values of the existing material. The syntax of material statement is written as

MATERIAL <LOCALIZATION> <MATERIAL_DEFINITION>

The localization can be defined by region if for example the same material constitutes several but with different parameters such as semiconductor with different alloy composition, or it can be done with material statement, for example

MATERIAL MATERIAL=INP AFFINITY=4.38

The material properties of InP given in chapter 1 and the parameters of the physical model given in section 2.1 that can be defined in material statement is listed in the next table.

Table.2.1 The parameters of material statement used in the simulation

Affinity	Specifies the electron affinity.
Arichn, Arichp	Specifies the effective Richardson constant for electrons and holes.
Edb	Specifies donor energy level.
Gcb	Specifies the conduction-band degeneracy factor.
Augn, Augp	Specifies the auger coefficient for electrons and holes.
Eg300	Specifies energy gap at 300 K.
Egalpha, Egbeta	Specifies the alpha and beta coefficient for temperature dependence of bandgap.
Nc300, Nv300	Specifies the conduction and valence band density of state at 300 K.
Nc.f, Nv.f	Specifies the conduction and valence band density of state temperature dependence.
Me.tunnel, Mh.tunnel	Specify the electron and hole effective masses for tunneling used in the universal Schottky tunneling model.
M.vthn M.vthp resistivity	Is an alias of electron and hole effective masses used to calculate the thermal velocity.
permittivity	Specifies relative dielectric permittivity of a material.
Resistivity	Specifies the material resistivity.
Drhod	Specifies the temperature coefficient of resistivity.

II. Specifying Physical Models:

Physical models are specified using the MODELS statement except impact ionization models which are specified using IMPACT statements. The parameters for these models appear on many statements including: MODELS, IMPACT, MOBILITY, and MATERIAL. The physical models can be grouped into five classes: mobility, recombination, carrier statistics, impact ionization, and tunneling. Some physical model Atlas activate them by default such as low filed mobility model and density of states temperature dependence with default material parameters, when the material parameters are defined in the MATERIAL statement Atlas use these parameters to calculates this physical models. Other physical models are activated when their material parameters are defined in the MAERIAL, CONTACT, or INTERFACE statements such as image force lowering and thermionic emission current. The MODEL statement used in this work is given as:

MODEL TEMPERATURE=180 FERMI SRH AUGER INCOMPLETE UST PRINT

TEMPERATURE: defined the lattice temperature where the parameters and the electrical characteristics will be calculated.
FERMI: activates Fermi-Dirac statistics
SRH : activates Schokcley-Read-Hall recombination.
AUGER: activates Auger recombination.
INCOMPLET: activates incomplete ionization of impurity.
UST: activates universal tunneling model.
PRINT: lists to the run time output the models and parameters, which will be used during the simulation. This allows the verification of models and material parameters.

III. Specifying Contact Characteristics:

An electrode in contact with semiconductor material is assumed by default to be ohmic. If a work function is defined in the CONTACT statement, the electrode is treated as a Schottky contact. The NAME parameter is used to identify which electrode will have its properties modified. The NUMBER parameter is used to define the electrode number in case there is several electrodes has the same name. Here will see the CONTACT statement parameters used in this work.

- WORKFUNCTION: used to define the metal work function that used as Schottky contact.
- SURF.REC: finite surface recombination which activate thermionic emission model.
- BARRIER: Turns on the barrier lowering for Schottky contact.

IV. Specifying Interface Properties:

The INTERFACE statement is used to define the interface charge density, surface recombination velocity at interfaces between semiconductors and insulators. Also, to define other parameters at the interface between other material such thermionic current between semiconductor-semiconductor. The interface statement can be written as

INTERFACE <LOCALIZATION> <PARAMETER>

The localization contain two parameters, the first parameter define the materials class constituting the interface (e.g. I.S which mean that the application of interface models specified

in this INTERFACE statement should include semiconductor-insulator interfaces). The second parameter define the material name constituting the interface, for example

INTMATERIAL= MATERIAL1/MATERIAL2.

c. Numerical method selection:

Different combinations of models will require Atlas to solve up to six equations. For each of the model types, there are basically three types of solution techniques: (a) decoupled (GUMMEL), (b) fully coupled (NEWTON) and (c) BLOCK. The GUMMEL method will solve for each unknown in turn keeping the other variables constant, repeating the process until a stable solution is achieved. The NEWTON method solve the total system of unknowns together. The BLOCK methods will solve some equations fully coupled while others are de-coupled.

Generally, the GUMMEL method is useful where the system of equations is weakly coupled but has only linear convergence. The NEWTON method is useful when the system of equations is strongly coupled and has quadratic convergence. The NEWTON method may, however, spend extra time solving for quantities, which are essentially constant or weakly coupled. NEWTON also requires a more accurate initial guess to the problem to obtain convergence. Thus, a BLOCK method can provide for faster simulations times in these cases over NEWTON. GUMMEL can often provide better initial guesses to problems. It can be useful to start a solution with a few GUMMEL iterations to generate a better guess. Then, switch to NEWTON to complete the solution. Specification of the solution method is carried out as follows:

METHOD NEWTON MAXTRAP=10

MAXTRAP parameters Specifies the number of times the trap procedure will be repeated in case of divergence. The value of MAXTRAPS may range from 1 to 10.

d. Solution specification:

Atlas can calculate DC, AC small signal, and transient solutions. Obtaining solutions is similar to setting up parametric test equipment for device tests. When a voltage is defined on an electrode in the device. Atlas then calculates the current through each electrode. Atlas also calculates internal quantities, such as carrier concentrations and electric fields throughout the device. This is information that is difficult or impossible to measure.

The solution is obtained by specifying the statement SOLVE INIT which gives an initial guess for potential and carrier concentrations from the doping profile which help to obtain convergence for the equation used.
the terminal characteristics calculated by Atlas is stored in log file by the next statement:
LOG OUTFILE=NAME.LOG
The bias sweep to calculate the DC and AC small signal can be done by the next statements respectively
SOLVE VANODE= 0.0 VSTEP= 0.1 VFINAL= 1.2 NAME= ANODE
SOLVE VANODE= 0.0 VSTEP= -0.1 VFINAL= -1.2 NAME= ANODE AC FREQ= 1E6

e. Results Analysis:

I. Tony plot:

TonyPlot is a graphical post processing tool for use with all Silvaco simulators and is an integral part of the VWF Interactive Tools. Tony Plot can operate stand-alone or along with other VWF Interactive Tools, such as DECKBUILD, VWF, or SPDB.
To plot a log file or several log file with tony plot the statement are respectively
TONYPLOT file1.LOG
TONYPLOT - OVERLAY file1.LOG file2.LOG

II. Extract:

The EXTRACT command provides within the DeckBuild environment allows to extract device parameters. EXTRACT operates on the previous solved curve or structure file. By default, EXTRACT uses the currently open log file. To override this default, supply the name of a file to be used by EXTRACT before the extraction routine. For example:
EXTRACT INIT INFILE="NAME.LOG"
In this work the EXTRACT statement was used to extract the square of reverse capacitance in pF and the current since the log file contain several data. The used EXTRACT statement for $1/C^2$-V and I-V are

- $1/C^2$-V

EXTRACT INIT INFILE="C.LOG"

EXTRACT NAME="1/C^2-V" CURVE

(V."ANODE",1/(C."ANODE""CATHODE"*1E12)^2) OUTFILE="1/C^2-V.DAT"

- I-V

EXTRACT INIT INFILE="I.LOG"

EXTRACT NAME="I-V" CURVE (V."ANODE",I."CATHODE"*-1) ="1/C^2-V.DAT"

OUTFILE="I-V.DAT"

Chapter 3
Extraction methods of Schottky diode parameters

3.1 Current-voltage methods

3.1.1 Standard method

The hypotheses of this method are:

A. $\emptyset_{b0}$ is determined from the saturation equation even if $n \geq 1$

B. $\emptyset_{b0}$ and n are voltage independent

C. equation (1.40) is approximated for $V_d = V - R_S \gg nkT/q$, and becomes:

$$I = I_s exp\left(\frac{q(V - R_S I)}{nkT}\right) \tag{3.1}$$

By deriving equation (3.1) as function to the voltage V, the ideality fact can be expressed as

$$n = \frac{q}{kT}\frac{dV}{dLn(I)} \tag{3.2}$$

Where $dV/d[Ln(I)]$ is the slope of region 2 in figure (3.1). The plot of *Ln (I)* VS. *V* remain a straight line as long as $V \gg nkT/q$ and $V \gg R_S I$.

The zero bias BH $\emptyset_{b0}$ can be calculated by rewriting the saturation current Equation as

$$\emptyset_{b0} = \frac{kT}{q} Ln\left(\frac{AA^* T^2}{I_s}\right) \tag{3.3}$$

The saturation current I_s is derived from the straight line intercept of $Ln(I)\ at\ V = 0$ as shown in figure (3.1).

This method is especially limited by the value of the series resistance, i.e. for high series resistance the region 2 shrinks and shows no linear regime. Another problem arises when

thermionic current is not the dominant transport mechanism, in this case $\emptyset_{b0}$ determined from equation (3.3) is only the result of calculation and has no real physical meaning [73]

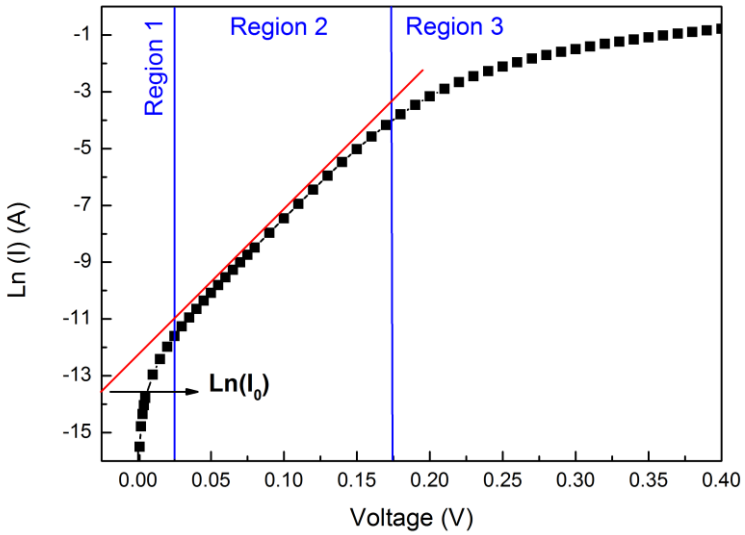


Figure 3.1: Typical I-V characteristic of Schottky diode.

3.1.2 Norde method

According to Norde [74] the problem with a series resistance can in many cases be avoided by using a plot of the function

$$F(V) = \frac{V}{2} - \frac{kT}{q} Ln\left(\frac{I(V)}{AA^{*}T^{2}}\right) \tag{3.5}$$

Equation (3.5) and equation (3.1) will give

$$F(V) = \emptyset_{b0} + IR_S - \frac{V}{2} \tag{3.7}$$

From equation (3.5), by plotting $F(V)$ as function of the voltage, the plot will be a straight line with negative slope ($F(V)$ decreases) in the bias range where the series resistance is neglected. Then $F(V)$ will start to increase as straight line in the bias range where the series resistance is dominated. The minimum of the $F(V)$ plot is the point of interest.

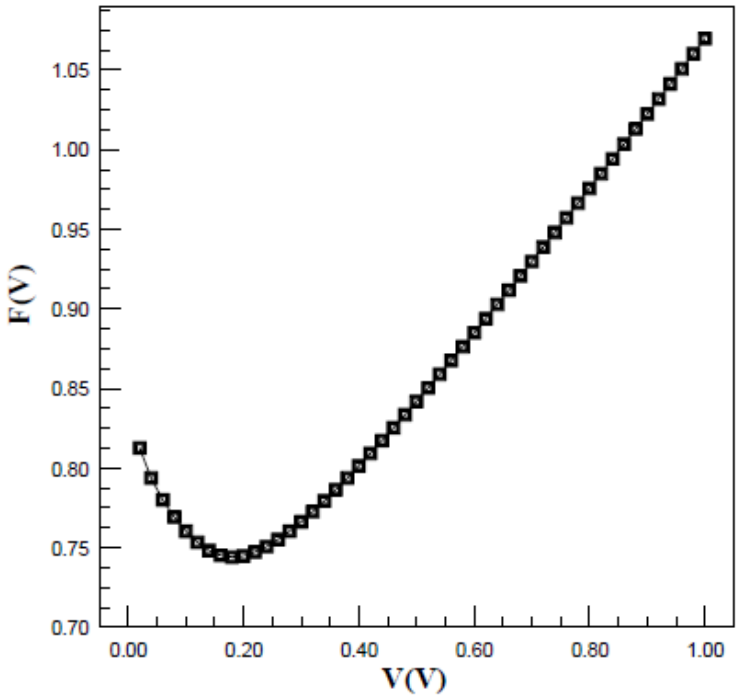


Figure 3.2: Example of F(V) vs. V plot from [75]

After some mathematical calculation, Norde derived $\emptyset_{b0}$ and R_S as function of $F(V_{min})$ which is the minimum of $F(V)$ plot, V_{min} which is the corresponding voltage to $F(V_{min})$ in $F(V)$ plot and I_{min} which is the current corresponding to V_{min} in the I-V characteristic.

$$\emptyset_{b0} = F(V_{min}) + \frac{V_{min}}{2} - \frac{kT}{q} \tag{3.7}$$

$$R_S = \frac{kT}{qI_{min}} \tag{3.8}$$

The Norde method was originally assumed the ideality factor n to be unity, thus for non-ideal diodes ($n > 1$) the series resistance is given by the expression [75,76]

$$R_S = \frac{(2-n)kT}{qI_{min}} \tag{3.9}$$

3.1.3 Cheung method

S. K. Cheung and N. W. Cheung in [77] proposed an alternate approach to determine the series resistance, the ideality factor and the zero bias BH from the I-V data using two plots. equation (3.1) can be rewritten in term

$$V = R_S I + n\emptyset_{b0} + \frac{n}{\beta} Ln\left(\frac{I}{AA^* T^2}\right) \tag{3.10}$$

Differentiating equation (3.10) with respect to I and rearranging terms, the next equation can be obtained

$$\frac{dV}{dLn(I)} = R_S I + \frac{n}{\beta} \tag{3.11}$$

By plotting dV/dLn (I) vs. I a straight line will be obtained as shown in figure (3.3). From equation (3.11), $R_S = \text{slop}$ and $n/\beta = \text{intercept}_{\text{Y.axis}}$.

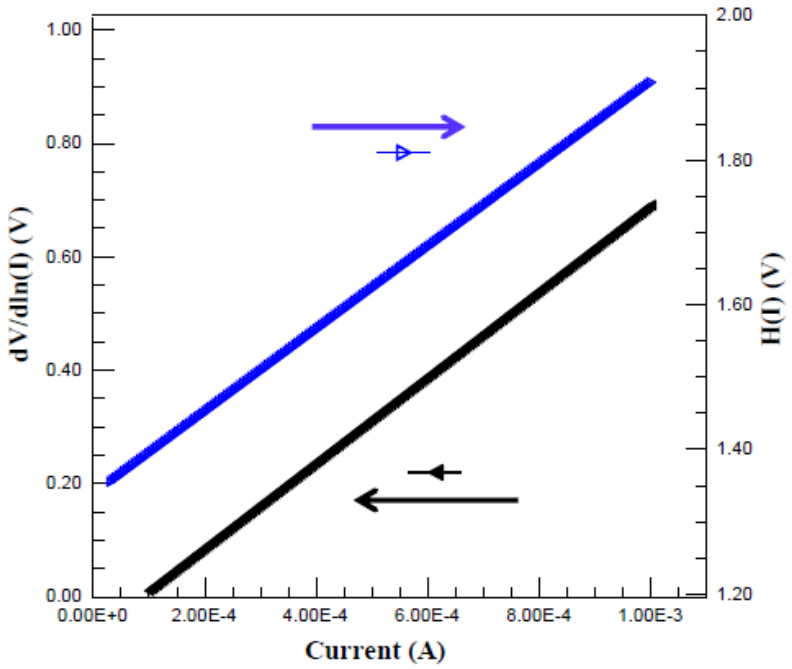


Figure 3.3: Example of *dV/d(lnI)* vs. *I* and *H(I)* vs. *I* plots from [75]

To evaluate $\emptyset_{b0}$, the authors define the function H(I):

$$H(I) = V - \frac{n}{\beta} Ln\left(\frac{I}{AA^* T^2}\right) \tag{3.12}$$

From equation (3.10)

$$H(I) = R_S I + n\emptyset_{b0} \tag{3.13}$$

Using equation (3.12) and the value of n determined from the previous plot the value of *H(I)* can be calculated. By plotting H(I) vs. I a straight line will be obtained as shown in figure (3.3). From equation (4.13), $n\emptyset_{b0} = \text{intercept}_{\text{ordinate}}$, The slope of this plot also provides a second determination of R_S which can be used to check the consistency of this approach.

3.2 Flat-band barrier height

The flat-band BH ($\emptyset_{fb}$) is a fundamental BH defined at a zero electric field and provides a better characterization of the physical barrier at the MS junction. The shift of the BH becomes zero at zero electric field since; at that point, there is no charge in the surface states. In addition the semiconductor bands are flat, precluding the tunneling and image force lowering from affecting the characteristics. The flat-band barrier height relates the zero-bias BH and ideality from an I-V measurement and is given by [78]

$$\emptyset_{fb} = n\emptyset_{b0} - (n-1)\frac{kT}{q}\ln\frac{N_C}{N_D} \tag{3.14}$$

If the flat band condition is certainly occurred and the extracted ideality value are correct, $\emptyset_{fb}$ should be constant. It appears that $\emptyset_{fb}$ is a fundamental BH and provides a better characterization of the physical barrier at the MS junction compared with $\emptyset_{b0}$.

3.3 Capacitance voltage method

The barrier height can also be determined from the C-V characteristic. By plotting the inverse of capacitance against the reverse voltage (plot of $1/C^2$ vs. V), the value of the barrier height can be obtained by the next equation [34]

$$\emptyset_{\text{CV}} = \text{V}_{\text{bi}} + \text{V}_{\text{n}} + \frac{\text{kT}}{\text{q}} \tag{3.15}$$

Where $V_{bi} = V' + (kT/q)$, and V' is s the extrapolation to the voltage axis such that $1/C_d = 0$ as shown in figure (3.4).

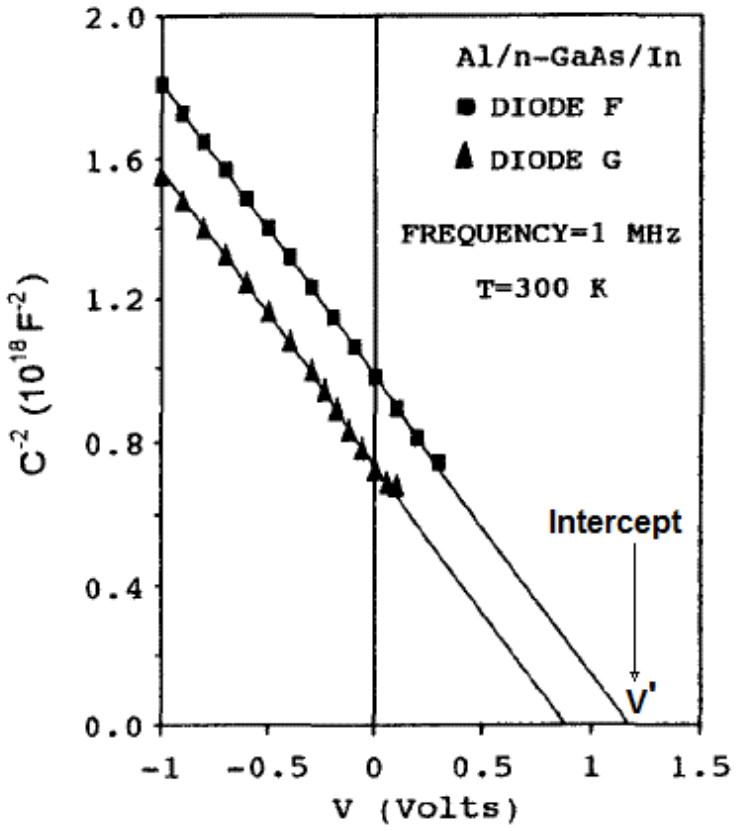


Figure 3.4: $1/C^2$-V plot for two Al/n-GaAs two Schottky diodes deposited by two different methods [79]

The CV method also measures the same fundamental barrier as the flat-band and should be equal in ideal Schottky junction, since $\emptyset_{CV}$ is an extrapolation to zero electric field [79].

3.4 Activation energy measurement

The principal advantage of SBH determination by means of an activation energy measurement is that no assumption of electrically active area is required, in contrary to the other methods. Because in some case the active area can be larger or smaller than the assumed area, or may be not known [34]. The activation energy measurement is based on the plot of Ln (I_S / T^2) vs. 1/T which called Richardson plot.

Richardson plot can be obtained by rewriting the saturation current equation as

$$Ln\left(\frac{I_s}{T^2}\right) = Ln(AA^*) - \frac{q\emptyset_{b0}}{kT} \qquad (3.16)$$

The plot is supposed to be linear where the ordinate intercept at $10^3/T = 0$ yields Richardson constant for a known diode area ($Ln(AA^*) = \text{intercept}$) and the slope yields the activation energy which is $\emptyset_{b0}$ ($-q\emptyset_{b0}/k = \text{slope}$). For non-ideal Schottky diode which have a temperature dependent BH Richardson constant will be found far away from the theoretical value. In addition Richardson plot of the most experimental studies Richardson plot deviate from linearity in low temperature as shown in figure (3.5), in this case the slope and the intercept is determined by the linear fitting of the linear region. The bowing of Richardson plot and the discrepancy between theoretical and obtained value of Richardson constant are a result of the BH dependence on temperature, and as discussed in the previous chapter the variation of the BH was interpreted in the experimental studies by BH inhomogeneities based on Werner and Guttler model or Tung model, thus Richardson plot is usually modified or corrected using the previous two models.

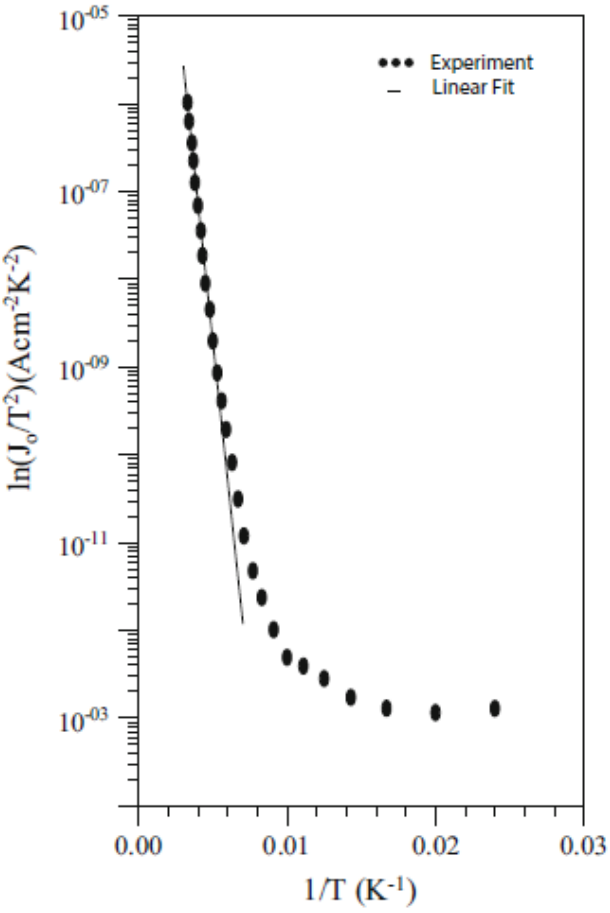


Figure 3.5: Example of Richardson plot from [80]

3.4.1 Modified Richardson plot with Werner and Guttler model

The modified Richardson plot relation is obtained by rewriting the saturation current equation from Werner and Guttler model (equation 1.53) [20-23]

$$Ln\left(\frac{I_s}{T^2}\right) - \left(\frac{q^2\sigma_0^2}{2k^2T^2}\right) = Ln(AA^*) - \frac{q\overline{\emptyset}_{b0}}{kT} \tag{3.17}$$

The values of σ_0 are obtained from the plot of $\emptyset_{b0}$ vs. 1/2kT (figure 3.6)**.** The plot should be a straight line where the intercept at ordinate gives the mean barrier $\overline{\emptyset}_{b0}$ ($\overline{\emptyset}_{b0}$ = intercept) and the slop gives the standard deviation of the Gaussian distribution of the BH ($-\sigma_0^2$ = slope) according to equation (1.51). If the plot is mot linear in some temperature range, the model should not be used to interpret the data in that temperature range.

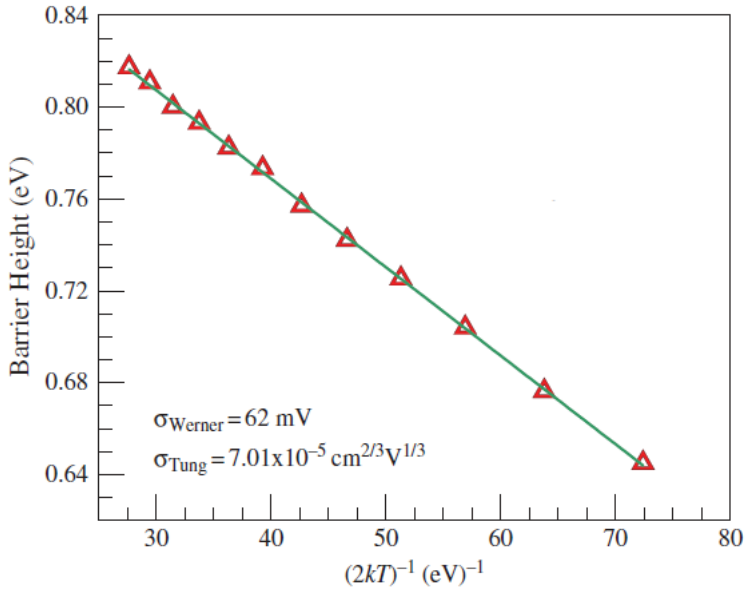


Figure 3.6: Example of $\emptyset_{b0}$ vs. 1/2kT plot from [81]

As shown in figure (3.7) the modified Richardson plot has a straight line where the intercept at ordinate yields A^* ($Ln(AA^*)$ = intercept) and the slop yields the mean barrier $\overline{\emptyset}_{b0}$ ($-q\overline{\emptyset}_{b0}/k$ = slope). When A^* and $\overline{\emptyset}_{b0}$ found in good agreement with the theoretical A^* and $\overline{\emptyset}_{b0}$ from $\emptyset_{b0}$ vs. 1/2kT plot respectively, the diode parameter temperature dependence explained based on BH Gaussian distribution of Werner and Guttler model [20-23]. The disadvantages of this modified Richardson plot are: σ_0 should be taken from the plot of $\emptyset_{b0}^c - \emptyset_{b0}$ vs. 1/2kT not from $\emptyset_{b0}$ vs. 1/2kT plot. Secondly $\overline{\emptyset}_{b0}$ taken from modified Richardson plot should be compared

with $\emptyset_{b0}^{c}$ not with $\overline{\emptyset}_{b0}$ from $\emptyset_{b0}$ vs. 1/2kT plot. Finally the area used to calculate A^* from the intercept is the area of the entire contact not the area of the small regions with low BH.

3.4.2 Modified Richardson plot with Tung model

From the total current equation of Tung model equation (1.67) we can write the saturation current of patches as

$$I_s = A_{eff} A^* T^2 exp\left[-\beta\left(\emptyset_{b0} - \frac{\sigma_1^2}{2kT}\left(\frac{V_{bb}}{\eta}\right)^{2/3}\right)\right] \tag{3.18}$$

The modified Richardson plot relation can be obtained by rewriting equation (3.18) [80-82]

$$Ln\left(\frac{I_s}{A_{eff}T^2}\right) - \frac{\sigma_1^2 {V_{bb}}^{\frac{2}{3}}}{2k^2T^2\eta^{\frac{2}{3}}} = Ln(A^*) - \frac{q\emptyset_{b0}}{kT} \tag{3.19}$$

The values of σ_1^2 are obtained from the plot of $\emptyset_{b0}$ vs. 1/2kT (figure. 3.6)**.** According to equation (1.68), the intercept at ordinate gives the homogeneous barrier $\emptyset_{b0}$ ($\emptyset_{\boldsymbol{b0}} = \text{ntercept}$) and the slop gives the standard deviation σ_1^2 of the patch parameter γ ($-\sigma_1^2\left(\frac{V_{bb}}{\eta}\right)^{2/3} = \text{slope}$). From equation (1.67) $A_{eff} = A\, C_1 A_p$, the area of the entire Schottky contact A is known. The effective area of one patch A_p can be determined from equation (1.71) at each temperature. The value of the patches density C_1 must be adjusted until the intercept modified Richardson plot (figure.3.7) gives a Richardson constant value in good agreement with the theoretical value ($\text{Ln}(A^*) = \text{intercept}$)**.** The slop yields the homogenous barrier $\emptyset_{b0}$ ($-q\emptyset_{b0}/k = \text{slope}$), $\emptyset_{b0}$ also must be in good agreement with $\emptyset_{b0}$ determined from $\emptyset_{b0}$ vs. 1/2kT plot.

In literature, the value of C_1 was found in [80, 26] for Schottky contact based on n-InP between (5.85×10^6 and $2.5 \times 10^{10}\ cm^{-2}$), for Schottky contact based on n-GaAs between (3.6×10^7 and $1.2 \times 10^{12}\ cm^{-2}$) in [82, 24] and between (2×10^8 and $5.5 \times 10^9 cm^{-2}$) for Schottky contact based on 4H-SiC in [28, 83].

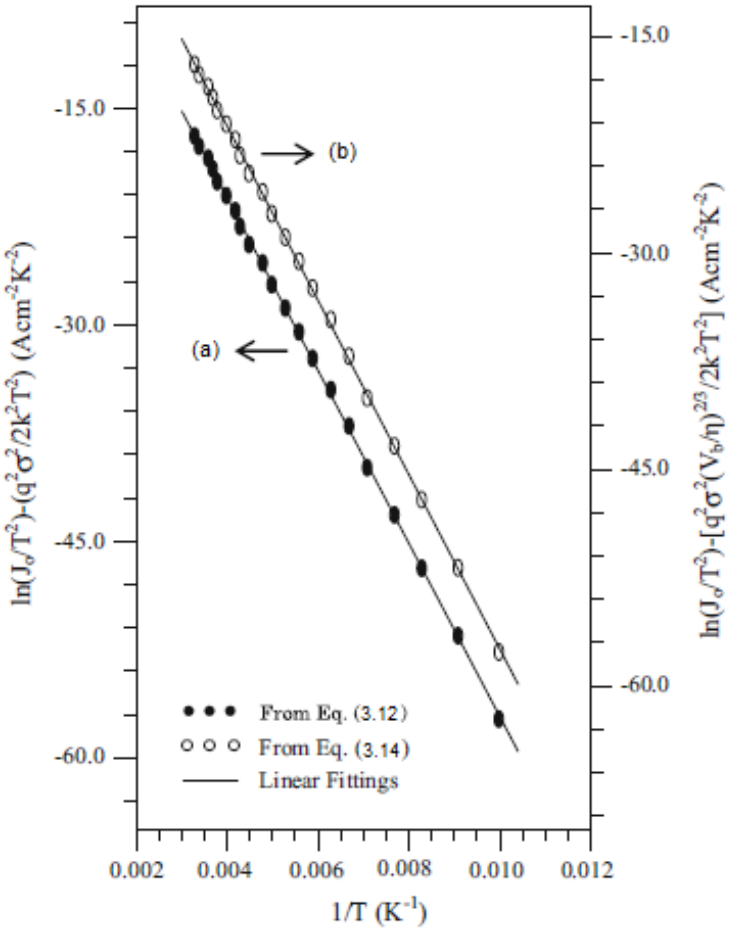


Figure 3.7: Example of modified Richardson plot with: (a) Werner and Gutller model, (b) Tung model, from [80].

Chapter 4
Results and discussion

4.1 Analyzing of experimental results

The temperature dependent behaviour of $\emptyset_{b0}$ *and* n for the experimental Au/n-InP SBD was explained according to Werner and Guttler model in the whole investigated temperature range (300-60 K). The disadvantages of Werner and Guttler model discussed in the second and the third chapters is a good reason to start this work by checking the validity of this interpretation. The experimental values of $\emptyset_{b0}$ in the investigated temperature range was fitted by the Gaussian distribution of the BH (equation 1.51). Thus we used these $\emptyset_{b0}$ values with thermionic emission current to simulate the I-V characteristic in two temperatures, 300 k (high temperature) and 160 K (low temperature), the results are shown in figure (4.1).

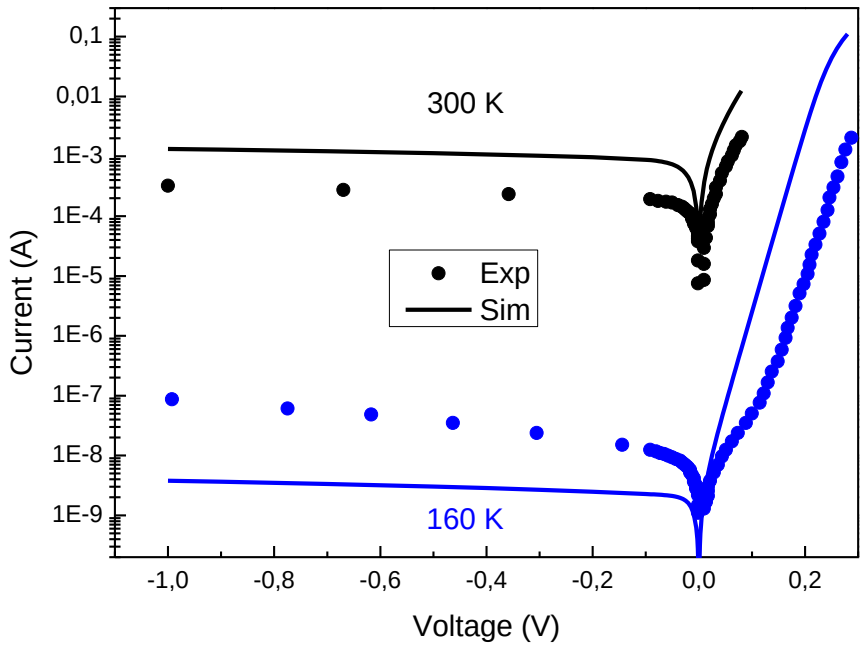


Figure 4.1: The experimental and simulated current voltage characteristic at 300 and 160 K.

As shown in the previous figure, the simulated characteristics does not fit the experimental ones. Even if the simulation was fitted the measurements, the interpretation based on this model still not valid, because the area used in this model is the total area of the Schottky contact. I.e. the investigation of Schottky contacts interface with spectroscopy measurements such as AFM (atomic force microscopy) [84] indicate that the average area of the small regions with low SBH is $7 \times 10^{-12}\ cm^{-2}$. As seen the mathematical agreement between the experimental $\emptyset_{b0}$ values obtained from I-V-T characteristics and equation (1.51) did not explain the BH temperature dependence. The second result needs to be analyzed is Richardson plot, because it shows an abnormal deviation from linearity in low temperature. Tung in [16] used his model to calculate the I-V-T characteristics of Schottky diode with inhomogeneous BH, he found that Richardson plot of such diode deviate from linearity in low temperature. Thus we assume that the BH inhomogeneity did not affect at least the high temperature (above 200 K) I-V-T characteristics.

4.2 High temperatures I-V characteristics

Since we assumed that the BH inhomogeneity did not affect the I-V characteristics we need to found the phenomena that causes the Schottky diode parameters temperature dependence. Thus we chosen to start from ideal case to know the difference between the experimental and ideal I-V-T characteristics, which gives us an idea about the physical models that should be used to regenerate the experimental I-V-T characteristics, for example, if the experimental I-V-T characteristics are lower than the ideal I-V-T characteristics, interface states is possibly the responsible.

4.2.1 Near Ideal diode

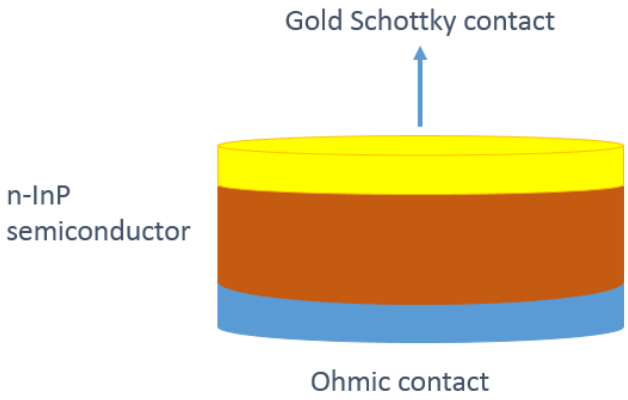


Figure 4.2: The structure of the near ideal diode.

In this section, the simulated diode structure is ideal and does not contain interface state and deep traps. As seen in figure (4.2) a circular gold Schottky contact with 1mm diameter was deposited on the top of n-InP semiconductor substrate with a thickness of 360 μm while a low resistance ohmic contact was deposited on the bottom of the sample.
Since we will simulate a near ideal SBD, the universal Schottky tunneling model described in the second chapter will not be used in contrary to all the other physical models which will be used here and in next sections.

a. Choosing the work function value

As seen in previous chapter the work function of gold have two values in literature, here we try to find which value is more appropriate. Figure (4.3) shows the simulated current voltage characteristic of the ideal diode at 300 K with the two work function values. The simulated I-V characteristic with Φ_M = 5.2 eV is lower than the experimental one with 5 order of magnitude, obviously there is no physical phenomenon can raises this current with five order of magnitude. On the other hand the simulated I-V characteristic with Φ_M = 4.8 eV greater than the experimental one with 1.4 order of magnitude, this order of difference can be avoided by using interface states.

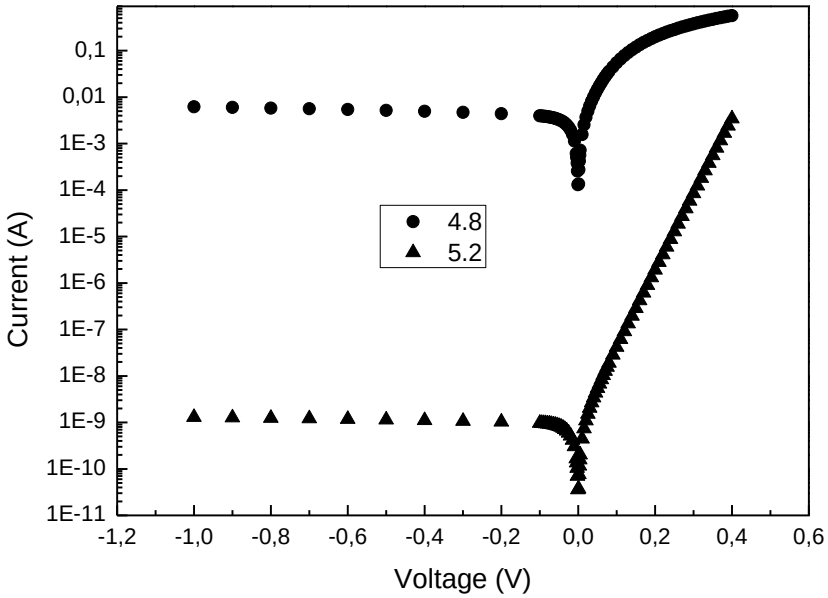


Figure 4.3: The simulated current voltage characteristic at 300 K of the ideal diode for different work function.

b. Effect of temperature

Figure (4.4) shows the I-V characteristics of the simulated Au/n-InP of the near ideal Schottky diode in the temperature range of 200-400 K by step of 20 K in semi-logarithm scale. The simulated current is found to be greater than the experimental current by 1.2 and 1.4 order of magnitude in temperature range of 200-300 K, when the temperature come close to 400 K we observe a large leakage current, which is a result of the littleness of the BH and the effect of the temperature on the reverse current.

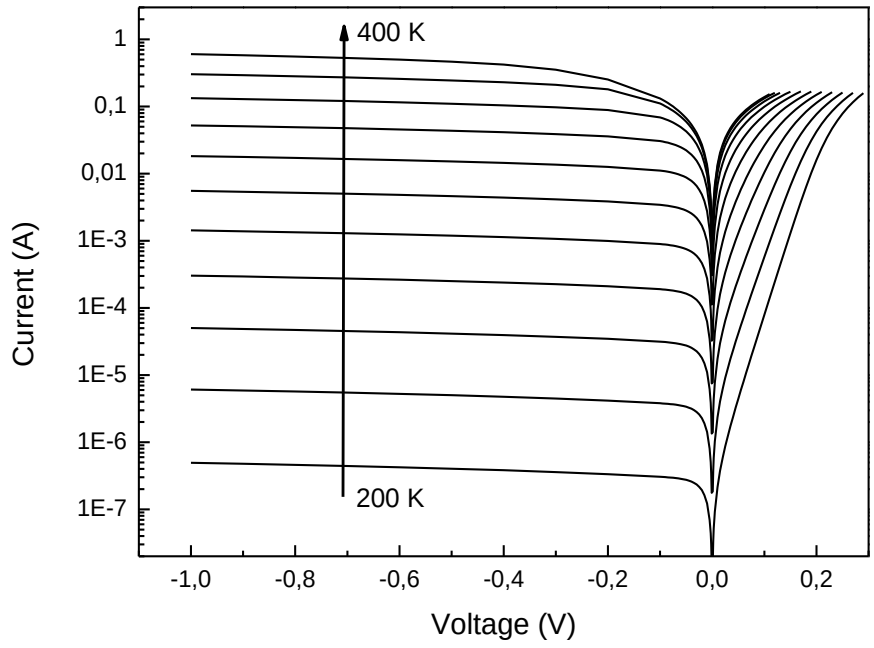


Figure 4.4: The simulated semi-logarithmic current-voltage characteristics of the ideal diode at various temperature range.

c. Parameter extraction

Using the parameters extraction current voltage methods illustrated in chapter 3, the diode parameters were extracted. Figure (4.5) and Figure (4.6) shows the two Cheung's plots and F(V) plot of Norde method respectively.

The obtained values of the Schottky barrier height and the ideality factor as a function of temperature are shown in table.4.1. As can be seen, the n values deviate from unity and shows a temperature dependence (increase with standard method and decrease with Cheung's method), such a behavior can be attributed to the voltage drop across the large series resistance. As it is well known the ideality factor is obtained from the linear region before the region where

the curve is strongly affected by the voltage drop across the series resistance. This linear region shrinks and shows more nonlinear regime with increasing temperature due to the increase of the series resistance. On the other hand the $\emptyset_{IV}$ values are temperature independent and shows a good agreement between the three methods.

Table 4.1: The extracted n and $\emptyset_{b0}$ values of the near ideal diode with different methods in temperature range 400-200 K.

Temp (K)	n		$\emptyset_{b0}\ (eV)$		
	standard	Cheung	standard	Cheung	Norde
400	3.14	0.18	0.426	0.422	0.435
380	2.24	0.30	0.415	0.410	0.417
360	1.87	0.40	0.400	0.405	0.399
340	1.59	0.65	0.388	0.392	0.387
320	1.38	0.80	0.381	0.390	0.382
300	1.25	0.90	0.382	0.386	0.382
280	1.16	0.95	0.384	0.386	0.383
260	1.03	1.0	0.389	0.390	0.384
240	1.02	1.0	0.390	0.393	0.392
220	1.02	1.0	0.395	0.396	0.398
200	1.02	1.0	0.398	0.400	0.400

Figure (4.7) shows the series resistance values extracted from the H(I) and dV/dLn(I) plots of Chueng's, and the calculated ones with Norde method using equation (3.8) (n =1) and equation (3.9) (with ideality factor from Cheung's method). The R_S values obtained from the two Cheung's plots are in good agreement, which prove the consistency of the method. While the values obtained from Norde method are close except below 300 K, while above 300 K when the ideality factor deviates from unity, the series resistance values shows an important disagreement with the values obtained by Cheung's method because equation (3.8) takes the ideality factor to be equal to 1. The values extracted with Cheung's method found to increase with increasing temperature. On the other hand the values extracted with Norde method did not increase with increasing temperature above 300 K due to the discrepancy between the ideality factor of the near ideal diode in the temperature range and the unity value of ideality factor used in Norde method.

As seen in table (4.1), n and $\emptyset_{b0}$ does not show a temperature dependence behavior in the range 200-300 K, also the simulated I-V characteristics are far away from the experimental ones. Therefore, other phenomena should be considered.

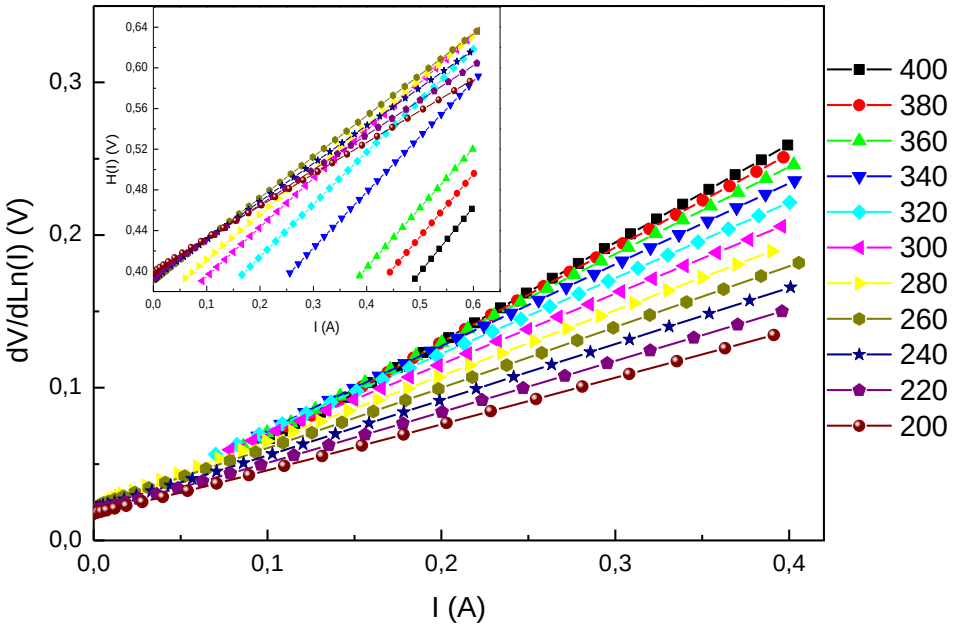


Figure 4.5: The plot of dV/d(LnI) versus I (insert figure: plot of H(I) versus I) of the near ideal diode in the temperature range 400-200 K.

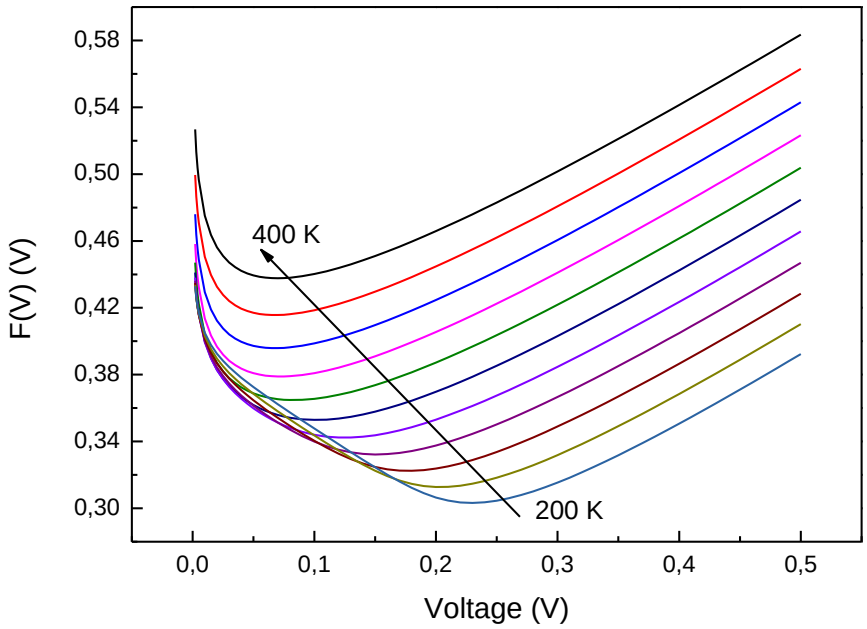


Figure 4.6: The F(V) versus V plot of the near ideal diode in the temperature range 400-200

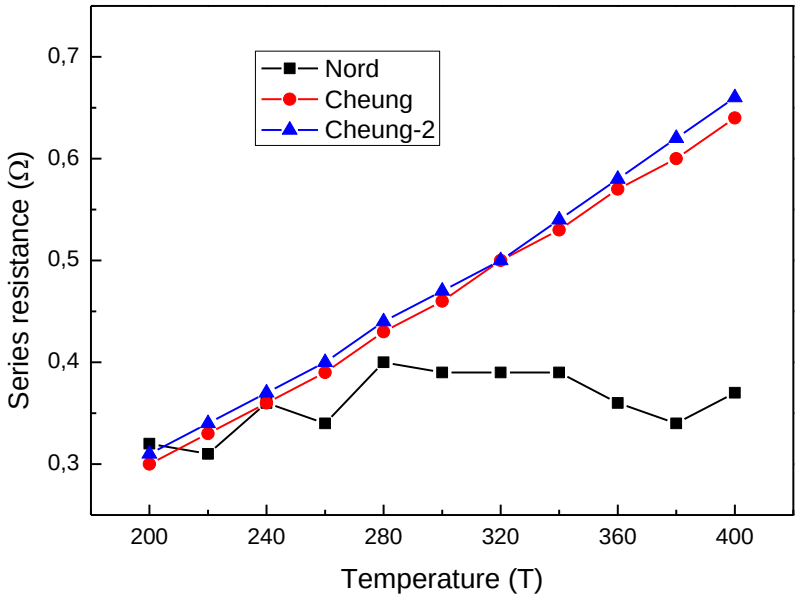


Figure 4.7: The series resistance of the near ideal diode calculated with various methods in the temperature range 400-200 K.

4.2.2 Real diode:

The simulated I-V characteristics in the temperature range 200-300 K were found greater than those from experiment by 1.4 to 1.2 order of magnitude, thus we must consider the presence of interface states in the experimental sample, since it plays a passivation role especially native oxide which have been reported by several works for n-InP.

To reproduce the main diode parameters temperature dependence behavior and acquire the experimental results the diode structure will be modified to contain at the MS interface a thin native oxide layer with a permittivity of 7.9 ε_0, positive charge between the n-InP substrate and the native oxide layer [10,11], the thickness will be varied between 5 and 20 Å. The new structure is shown in figure (4.8).

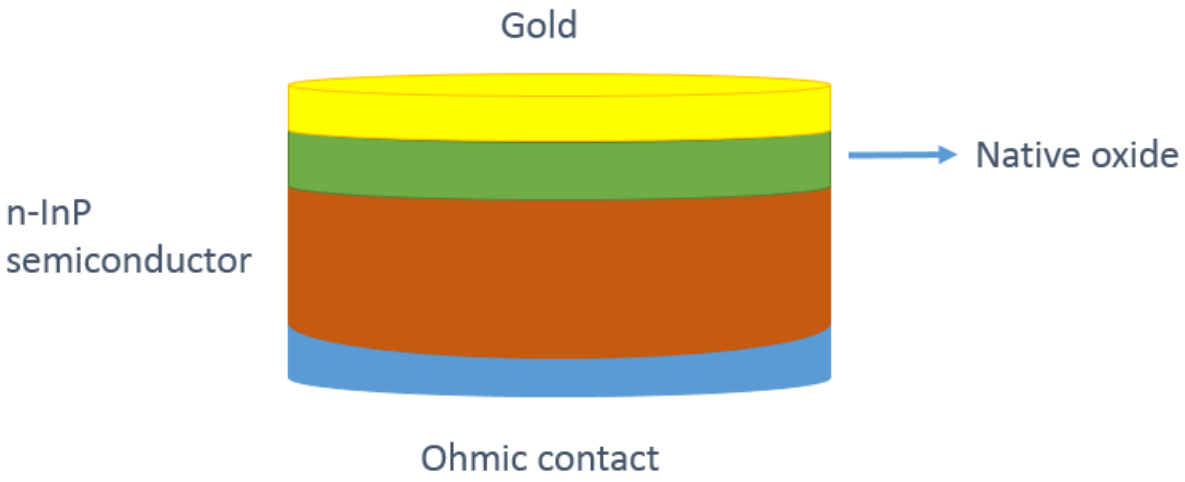


Figure 4.8: the structure of the real diode.

a. Native oxide

As seen in figure (4.9) native oxide layer thickness has a reverse relation with current, i.e. as the thickness increase the current decrease. In addition, the presence of a thin native oxide layer at the MS interface causes a peak at the forward bias, this peak is eliminated by the positive interface charge, since the I-V characteristics represented in figure (4.9) was simulated without the positive interface charge, to show its effect.

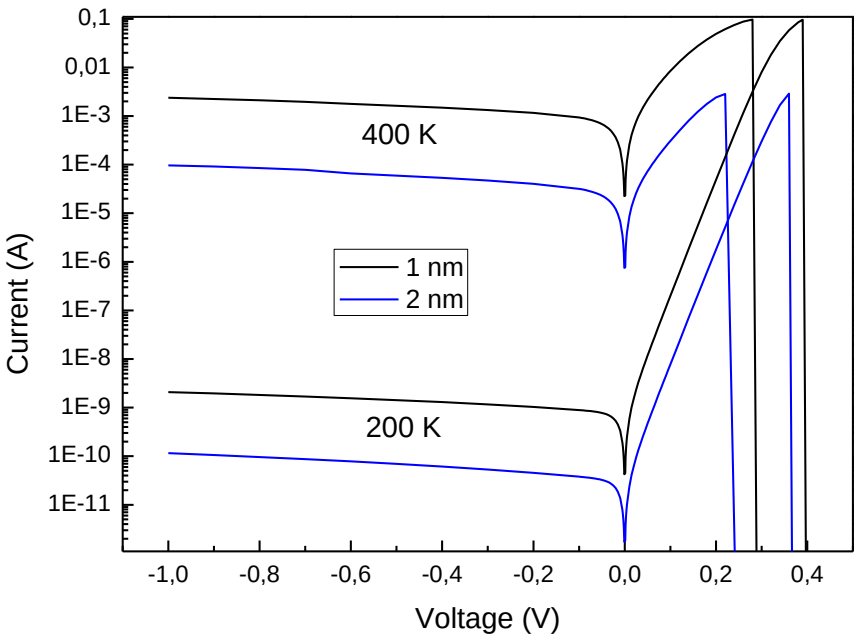


Figure 4.9: Native oxide layer effect on current transport process.

Since the electron does not have a sufficient energy to surmount the high potential across the interfacial layer. Hence thermionic emission current was eliminated. Thus we added another current transport process, which is quantum mechanical tunneling using universal Schottky tunneling model described in section 2.1.9. As a result, the transport conduction mechanisms are dominated by quantum mechanical tunneling through the barrier and the insulator layer in all the temperature range. In this case, when there is a thin insulator layer at the interface of the Schottky diode, the normalization of E_{00} (characteristic tunneling energy that is related to the tunnel effect transmission probability) to the thermal energy KT cannot be used to determine the dominant current processes, because there is no thermionic current to compare with tunneling current.

b. I-V-T characteristics

The final I-V characteristics of the real diode in the temperature range 200-400 K are shown in Figure (4.10). These results were obtained using a native oxide thickness equal to 5 Å and $6 \times 10^{11}\ cm^{-2}$ positive interface charge. As can be seen the leakage current in the high temperatures was reduced compared to the near ideal diode, which is attributed to the interfacial layer.

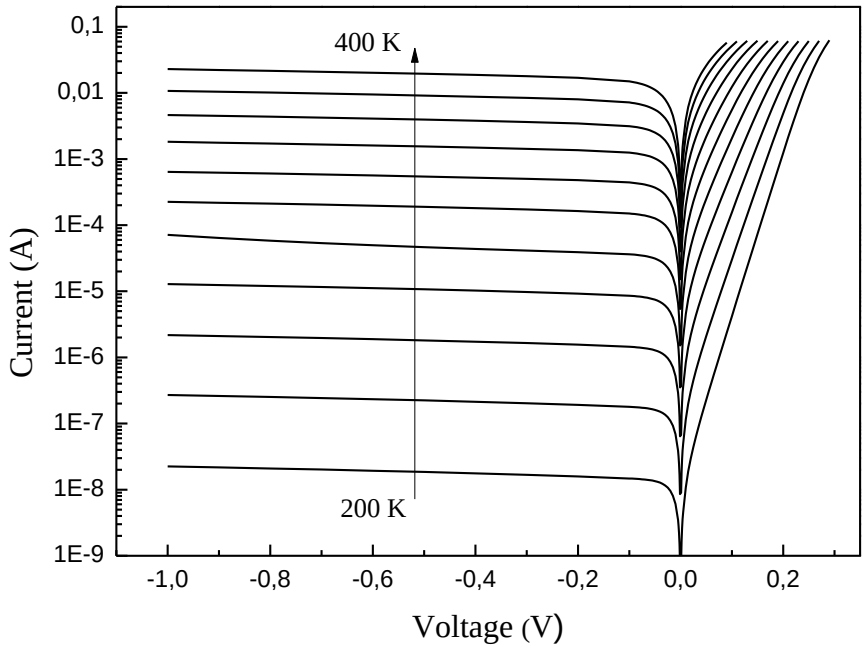


Figure 4.10: The Simulated semi-logarithmic current voltage characteristic of the real diode at various temperature range.

The obtained current is in very good agreement with the experimental current [85] in the temperature range 200-300 K as shown in figure (4.11). and figure (4.12).

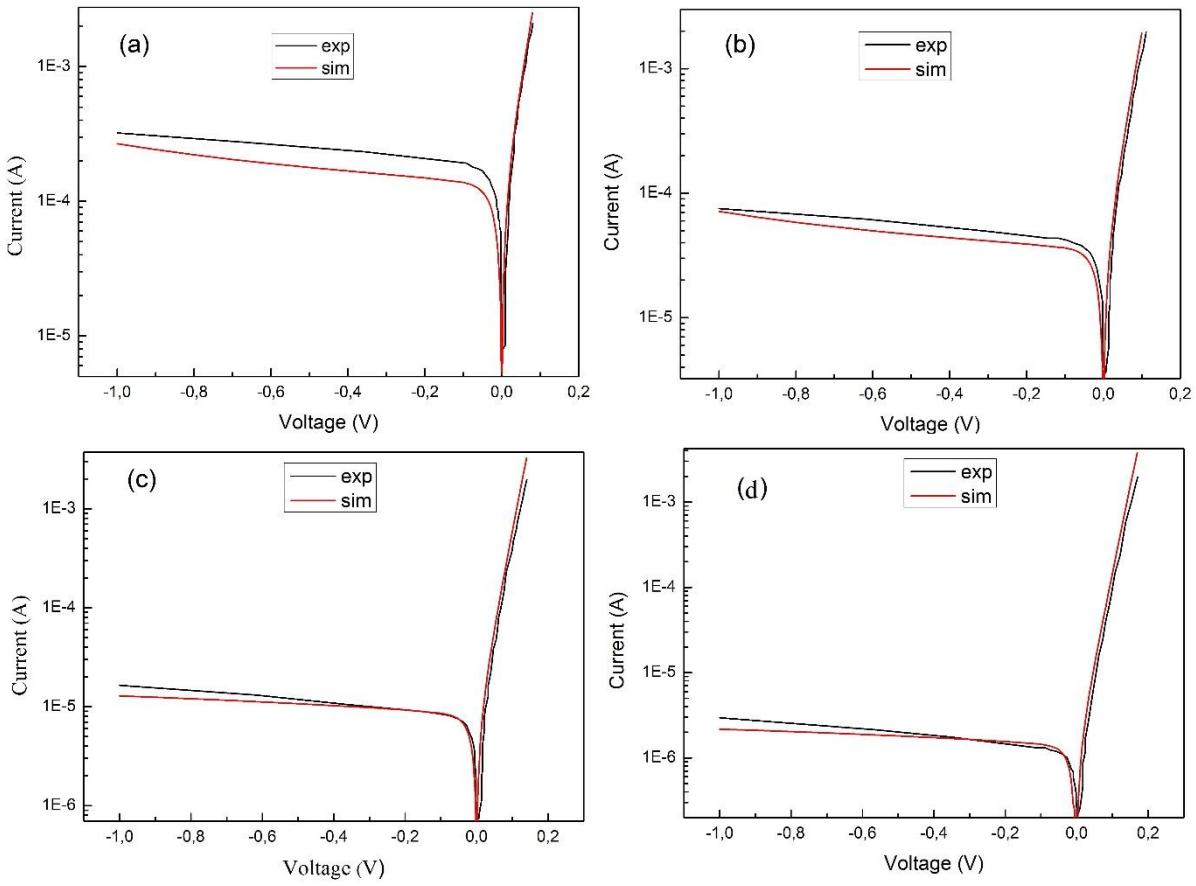


Figure 4.11: Comparison of the simulated I-V characteristics with measurement at: (a) 300 K, (b) 280 K, (c) 260, (d) 240.

Except the reverse current in the temperatures 220 and 200 K, where the experimental data shows a leakage current in contrary to simulation that failed to regenerate the leakage current and saturate immediately.

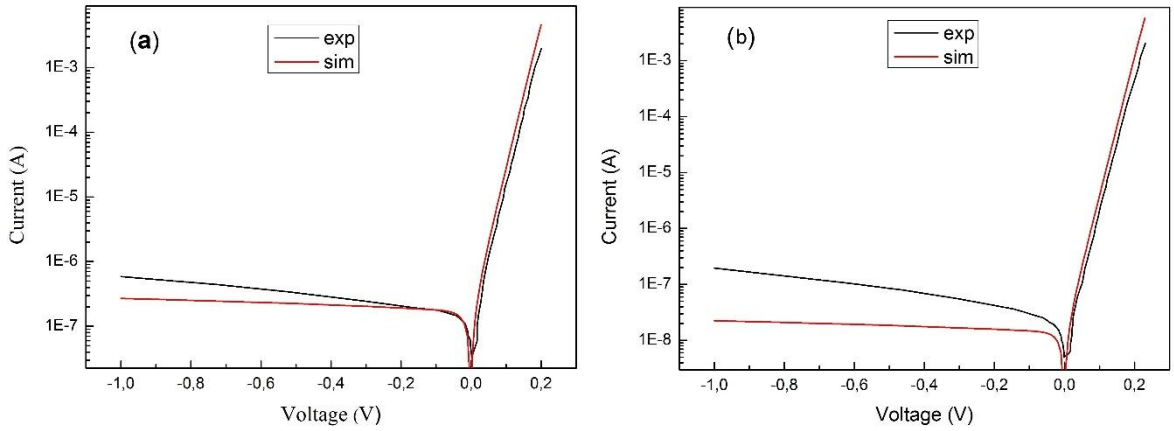


Figure 4.12: Comparison of the simulated I-V characteristics with measurement at: (a) 220 K, (b) 200 K.

c. Parameters extraction

The values of $\emptyset_{b0}$ and n are listed in table (4.2). The $\emptyset_{b0}$ values obtained by the three methods are higher than those of the near ideal diode, this is a result of diode passivation by the thin native oxide layer, this increase of $\emptyset_{b0}$ is an important advantage because it gives a better rectifying characteristics. n increased likewise in the temperature range 200-300 K, this effect of native oxide on $\emptyset_{b0}$ and n is in good agreement with [11, 86, 87]. Above 300 K the effect of high temperature on n observed in the near ideal diode was reduced since the series resistance of the real diode is lower than the ideal diode series resistance. Concerning the temperature dependence, both parameters extracted with the standard methods exhibits a temperature dependence above 300 K and they are ranged from 0.481 eV and 1.55 (at 400 K) to 0.465 eV and 1.02 (at 320 K), such behavior is due to the effect of series resistance in high temperature, while below 300 K almost constant. The extracted values in the comparison temperature range are not in a good agreement with the experimental ones which can be interpreted by the deference in the extraction region.

According to [23] the deviation of current conduction mechanism from TE theory resulting in a high value of the ideality factor which is not the case here, this is because tunneling current have the same slope of TE current. While the zero-bias BH shows a temperature dependence in the simulated temperature range because it was calculated using thermionic emission theory

and the saturation current values of tunneling current that dominates the transport mechanism and does not have the same saturation current of thermionic emission current.

Table 4.2: The extracted n and $\emptyset_{b0}$ values of the real diode with different methods in temperature range 400-200 K.

Temp (K)	n		$\emptyset_{b0}\ (eV)$		
	standard	Cheung	standard	Cheung	Norde
400	1.55	0.84	0.481	0.480	0.473
380	1.38	0.88	0.472	0.477	0.468
360	1.15	0.90	0.472	0.475	0.465
340	1.04	0.93	0.471	0.472	0.463
320	1.02	0.96	0.465	0.467	0.460
300	1.00	0.98	0.463	0.462	0.459
280	1.00	1.00	0.460	0.458	0.462
260	1.01	1.00	0.456	0.457	0.461
240	1.02	1.00	0.453	0.456	0.460
220	1.02	1.00	0.452	0.455	0.459
200	1.02	1.00	0.450	0.453	0.458

The values of $\emptyset_{b0}$ extracted with Cheung's method are almost identical to those extracted with standard method likewise the ideality factor in the temperature range 200–300 K, meanwhile $\emptyset_{b0}$ values extracted with Norde method exhibits less temperature dependence than those extracted by the standard and Cheung methods. The two Cheung plots and F(V) plot of Norde method are shown in figure (4.13) and figure (4.14) respectively.

As seen in figure (4.15) the series resistance values increase with increasing temperature and are lower than the values of the near ideal diode. As observed in vast number of papers the series resistance found to increase with increasing temperature when the I-V curves does not intersect [93- 96], on the other hand when the I-V curves intersect the series resistance found to decreasing with increasing temperature [92] like in our case.

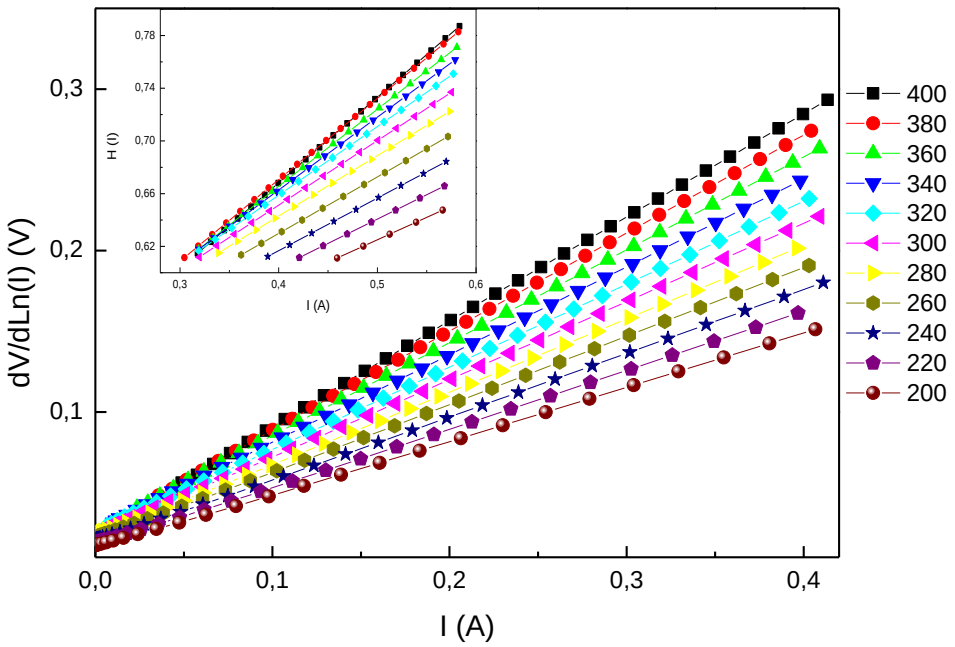


Figure 4.13: The plot of dV/d(LnI) versus I (insert figure: plot of H(I) versus I) of the real diode in the temperature range 400-200 K

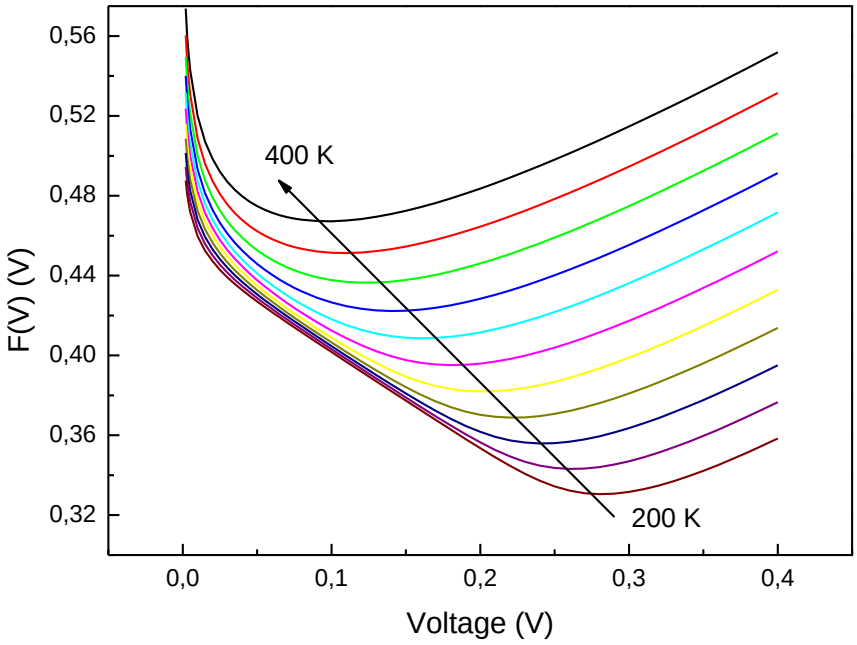


Figure 4.14: The F(V) versus V plot of the real diode in the temperature range 400-200.

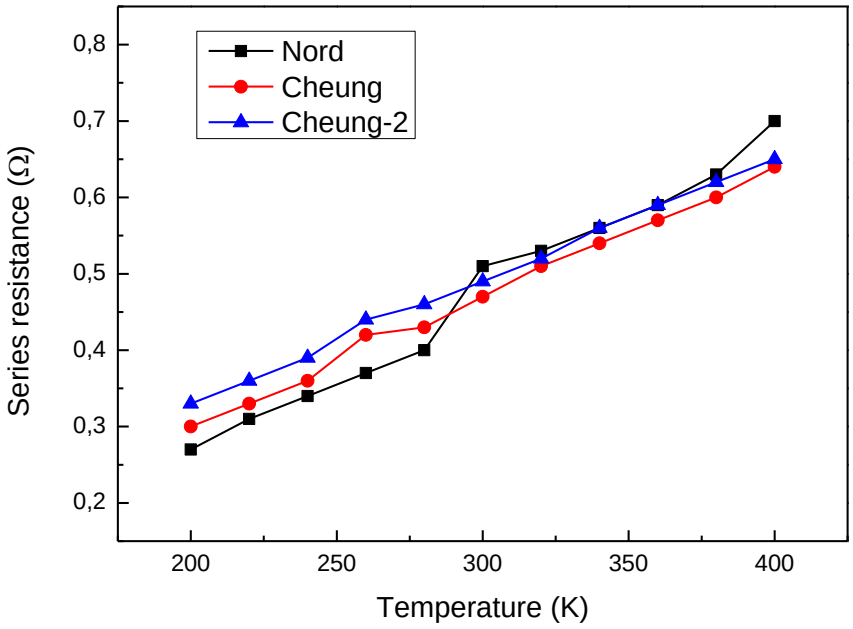


Figure 4.15: The series resistance of the real diode calculated with various methods in the temperature range 400-200 K.

d. Richardson plot

For more investigations on the non-ideal behavior of the forward-bias I-V characteristics, we show the conventional activation energy/Richardson plot of $\ln(I_0/T^2)$ vs. 1/T in figure (4.16). The plot is found to be linear in the simulated temperature range (200-400 K), similar result have been reported by Korucu et al. [23] in this temperature range. This linearity of the simulated Richardson plot is a consequence of the barrier homogeneity. While the linearity of the experimental Richardson plot indicates that the current flow through the uniform barrier is the dominant current in that temperature range, that is, when the temperature is lowered, the junction current is dominated by fewer low-SBH regions with lower effective SBH's [16]. An effective energy (E_a=0.334 eV) and Richardson constant (A^{**}=0.063 $AK^{-2}cm^{-2}$) were obtained. This value of E_a (0.334 eV) is lower than half of the energy band gap of InP semiconductor at 300 K, this confirms that the predominant conduction mechanism is not TE, since the activation energy of Richardson plot represent the effective BH. In addition, the value of Richardson constant A^{**}= (0.063 $AK^{-2}Cm^{-2}$) is lower than the known value (9.4 $AK^{-2}cm^{-2}$) for n-InP. This is a result of the SBH temperature dependence, due to the deviation of the transport conduction mechanism from thermionic emission theory.

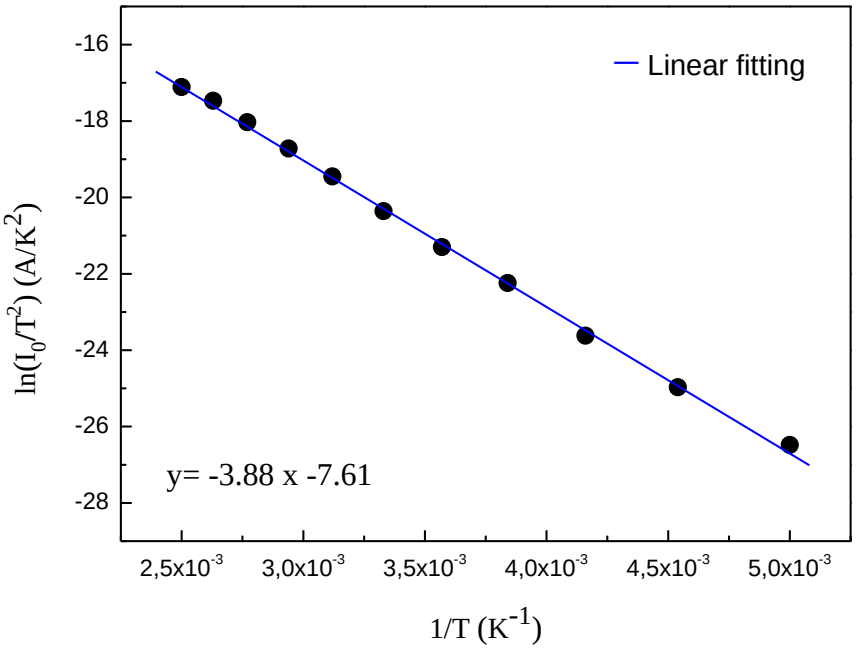


Figure 4.16: Richardson plot of $\ln(I_0/T^2)$ versus 1/T of the real diode.

4.3 Low temperatures I-V characteristics

In the previous section 4.2 the experimental current was regenerated successfully using interface states which is a thin native oxide with specific permittivity and thickness values in addition to tunneling current. The native oxide played a passive role by reducing the current as explained in section 4.2 (TE current was eliminated and replaced by TFE current which has lower density), but TFE current has been found insufficient to regenerate the experimental current bellow 200 K, in more details, in revers bias from 180 K and the low forward bias from 160 K, and the ratio of experimental current to TFE current continue to increase with the decrease of temperature.

This discrepancy between simulation and experimental current bellow 200 K support the hypothesis proposed in section 4.1 which suggest that the low temperature IV characteristics are dominated by the current flow through the low Schottky barrier regions. So, the lateral SBH inhomogeneity should be considered in the next section using Tung model.

4.3.1 Modified Richardson plot with Tung model

The objective from modified Richardson plot with Tung model is to determine the effective area of patches which is the only parameter that cannot be calculated with the mathematical equation given in section 1.3.2, the standard deviation was calculated using the slop of the experimental $\emptyset_{b0}$ vs. 1/2kT plot, while the saturation current is just taken from the experimental I-V characteristics. After the determination of A_{eff} of the patches the simulation of inhomogeneous SBD will be easier and more accurate. The calculated patches parameters are listed in table (4.3).

The extraction of the saturation current in low temperature where the current is affected by SB inhomogeneity have some details to discuss, the forward experimental I-V characteristics can be divided to two parts, the first part is the current in the bias range shown in the insert of Figure (4.17), this current represent the I-V characteristics of patches, while the second part is the I-V characteristics of the homogenous diode. In other words, the experimental I-V characteristics in low temperature and low forward bias (below the threshold voltage or less) is dominated by the current flows through small regions with low SB, where the current flows through the homogeneous barrier is dominated in the rest bias range.

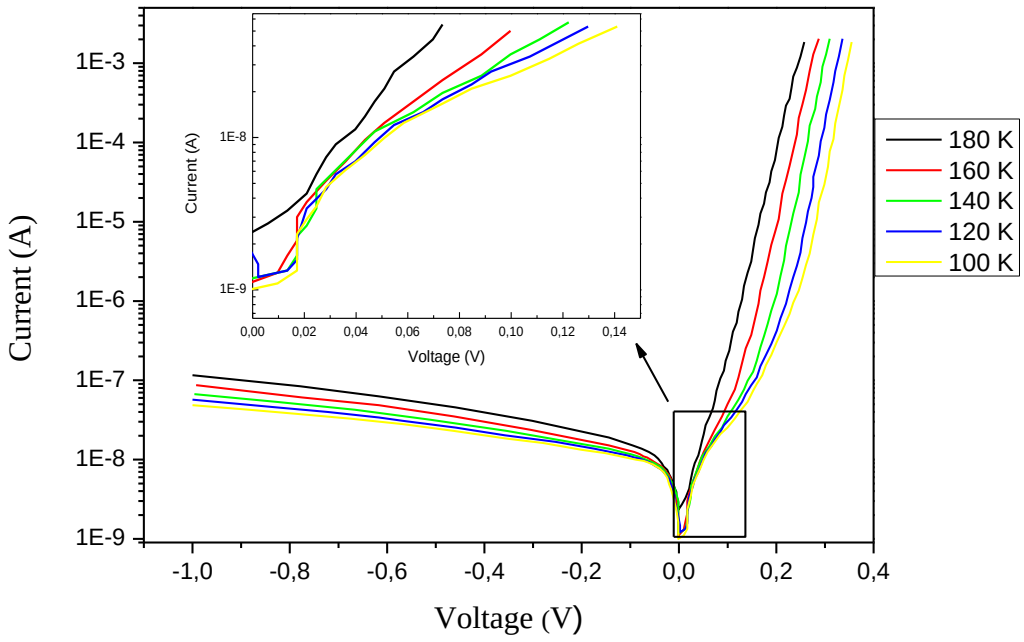


Figure 4.17: The experimental low temperature I-V characteristics (the insert show zoom-in on the effective patch bias region).

As seen in table (4.3), the values of saturation current were given just in two temperatures (180 and 160 K), the reason is that the experimental forward I-V characteristics of patches in the temperature range 160-100 K (in the insert of Figure 17) have almost the same saturation current, which means that the forward patches current in the temperature range 160-100 K has flown through patches that have the same Y parameter or in other word the same effective patch.

Table 4.3: Effective patch parameters used in modified Richardson plot.

T	V_{bb}	η	σ	Δ	A_p	C_1	A_{eff}	I_S
180	0.360	5.71E-5	7.08E-5	0.120	1.64E-11	2E6	1.29E-7	2E-9
160	0.367		7.04E-5	0.130	1.55E-11		1.22E-7	5E-10
140	0.373		7.00E-5	0.140	1.44E-11		1.13E-7	
120	0.380		6.95E-5	0.180	1.56E-11		1.22E-7	
100	0.387		6.91E-5	0.222	1.58E-11		1.23E-7	

The modified Richardson plot values shown in Figure (4.18) was calculated using the parameters listed in Table (4.3) and equation (3.19), the plot found to be a straight line where the intercept with ordinate yields Richardson constant which is the point of interest, and the slope gives the homogeneous barrier, where both must be in good agreement with the theoretical value of Richardson constant and the homogenous barrier value obtained from $\emptyset_{b0}$ vs. 1/2kT plot.

The best Richardson constant value (8.58 $AK^{-2}cm^{-2}$) was obtained with patches density $C_1 = 2E6\ cm^{-2}$ which is in good agreement with the theoretical value (9.4 $AK^{-2}cm^{-2}$). While the mean barrier where obtained equal to 0.39 eV which is close to the experimental one (0.52 eV). Now the simulation of low temperature I-V Characteristics can be performed using effective patches areas (A_{eff}) listed in table (4.3) and effective barrier height $\emptyset_{eff}$ values which are the two parameters needed to simulate inhomogeneous barrier with ATLAS-SILVACO software.

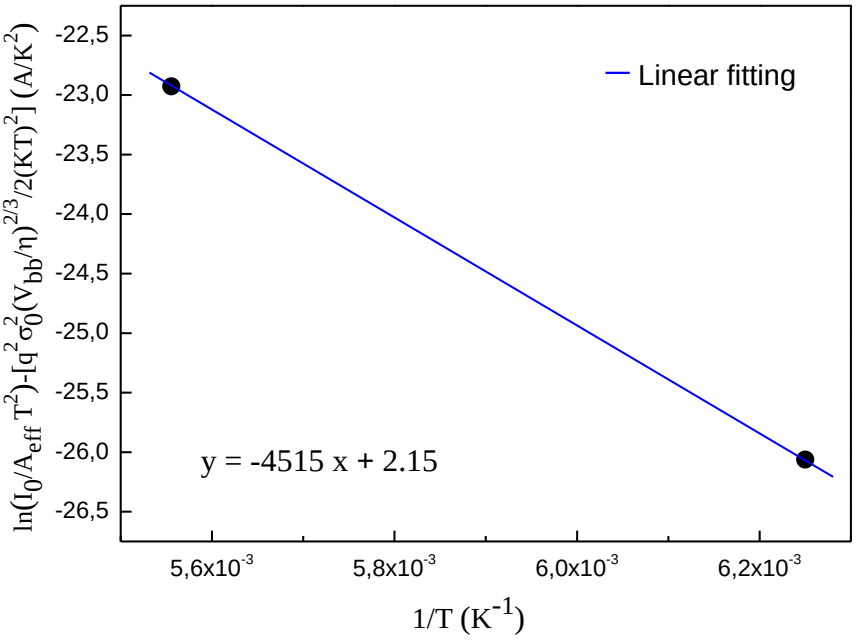


Figure 4.18: Modified Richardson plot with Tung model.

4.3.2 I-V-T characteristics:

The homogeneous structure of the real diode will be modified to contain a small circular region with lower barrier height and specific radius (figure 4.19). This region has the same InP substrate parameters except the affinity which will be increased to modify the barrier height of the small circular region of the effective patch.

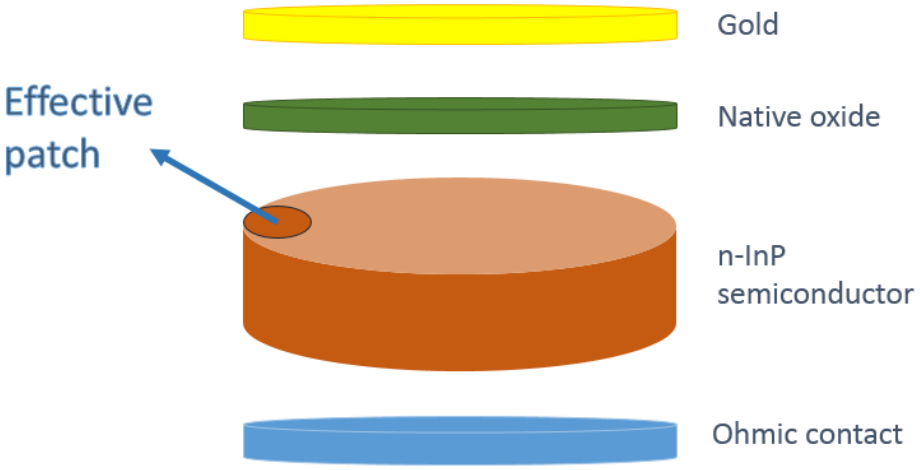


Figure 4.19: The structure of the inhomogeneous diode.

As discussed in the previous section, the simulation of inhomogeneous SBD based on Tung model need two parameters, the effective patches surface A_{eff} and their BH values. Using A_{eff} values listed in table (4.3) and effective barrier height $\emptyset_{eff}$values in the temperature range 180-100 K the I-V characteristics were simulated. In contrary to the expected results, the simulated I-V characteristics did not fitted the experimental I-V-T characteristics, the reverse and low forward bias current has been found so much lower than experimental ones and is similar to the current of the homogeneous SBD. This disagreement can be interpreted easily based on transport mechanism types, that is, the experimental barrier values were extracted based on TE theory while the dominated transport mechanism is tunneling as discussed in section 4.2.2.c, in addition Tung model equation also is based on TE theory. So, the A_{eff} values gotten from modified Richardson plot with Tung model and the experimental BH values used in simulation of the I-V characteristics in this temperature range are apparently not correct.

After the fail of simulation using the parameters extracted from Richardson modified plot and the experimental data the only rest solution is to carried out the simulation with the hard way.

The I-V characteristics must be simulated with modeling the barrier and effective area of patches in each temperature and in reverse and forward bias until it fits the experimental I-V characteristics, after thousands of simulation attempts, the true parameters of the effective patches which the current flows through in low temperatures are found and listed in table (4.4).

Table 4.4: The effective patch barrier and area used to regenerate the low temperature experimental I-V characteristics.

T	reverse		forward	
	Radius (μm)	Barrier (eV)	Radius (μm)	Barrier (eV)
180	0.02	0.02	/	/
160	0.02	0.02	0.1	0.1
140	0.02	0.02	0.1	0.1
120	0.02	0.02	0.1	0.1
100	0.02	0.01	0.1	0.1

From the last table is clear that the forward bias current in the temperature range 160-100 K flows through the same effective patch which is in consistence with the analysis of the experimental saturation current values in section 4.3.1. The effective patch has an effective area equal to $3.141 \times 10^{-10}\ cm^{-2}$ which represent $1/(2.5 \times 10^{8})$ of the total Schottky diode area, as for the barrier is equal to 0.1 eV which is a small barrier. On the other hand the reverse bias current in the temperature range 180-100 K flows through two effective patches with an

effective area less by 25 times than the forward effective patch area, also its barriers height have a very low value (0.02 eV in temperature range 180-100 K and 0.01 eV in temperature 100 K). The simulated I-V characteristics in the temperature range 180-100 K are shown in figure (4.20). In forward bias the current is dominated by electrons flows through the forward effective patch in the low bias range and this range increases with decreasing temperature, then the current is dominated by electrons flowing through the homogeneous barrier. In the reverse bias the current is dominated by electrons flowing through the revers effective patch. We must note that the effective patch used in the reverse bias simulation did not affect on the forward I-V characteristics and vice-versa for the patch used in the forward bias simulation and reverse I-V characteristics.

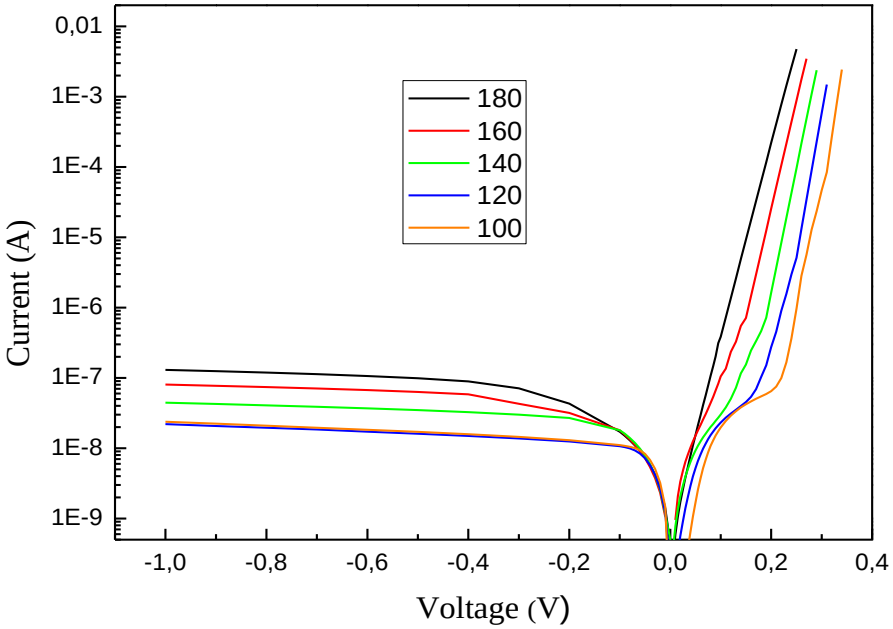
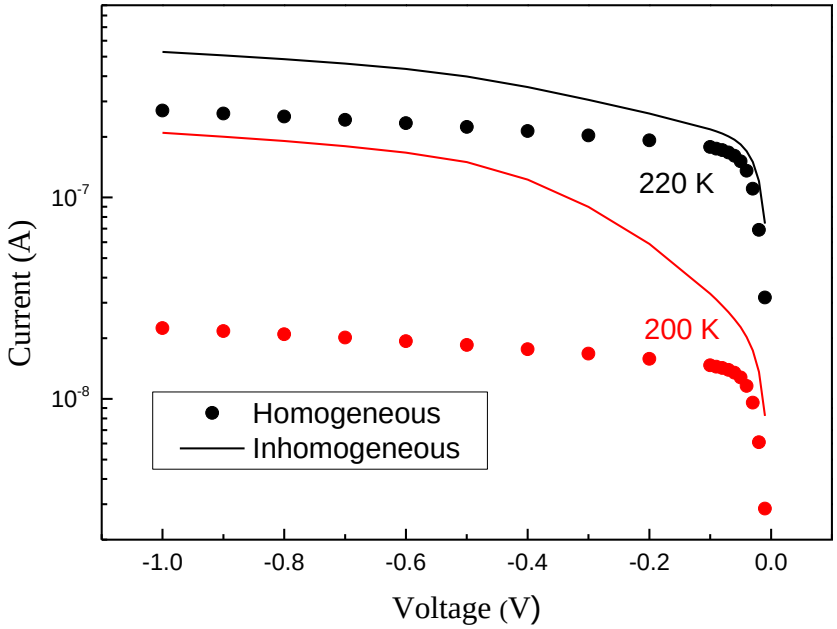


Figure 4.20: The simulated low temperature I-V characteristics with inhomogeneous SBD.

Another evidence support the low temperature simulation purpose is the reverse bias soft characteristics or leakage current. In more details, as seen in section.4.2.2.b, the experimental I-V characteristics did not truly saturate until 240 K and the simulated I-V characteristics with the homogeneous diode failed to regenerate this leakage current, whereas the simulated low temperature I-V characteristics with inhomogeneous diode was successfully reproduced this phenomenon observed in the experimental I-V characteristics in 220-200 K (Figure 4.21) as well in low temperature range.

The interpretation of the phenomenon is based on three concepts: - The littleness of the barrier height which is close to zero. – The barrier height at the metal side is constant in function of applied bias. – Finally the tunneling probability of Universal Schottky tunneling (UST) model depend on the electrical field. From the previous three concepts we can conclude the following: the reverse current flows through the homogeneous barrier do not shows a leakage current because the barrier height in the metal side is high enough to dominate over the electrical field in the tunneling probability of UST model, on the other hand the reverse current flows through the effective patch barrier shows a leakage current since the electrical field in the tunneling probability of UST model dominates over the small barrier value of the effective patch which makes the current depending on the reverse bias and increase as the reverse bias increases.



Fog 4.21: The simulated reverse current in 220 and 200 K with homogeneous and inhomogeneous SBD.

The new I-V characteristics simulated with inhomogeneous SBD are in close agreement with the experimental ones (Figure 4.22) in contrary to I-V characteristics simulated with homogeneous SBD.

The simulated low temperature I-V characteristics also are in close agreement with the measurement in reverse and forward bias as shown in figure (4.23 and 4.24).

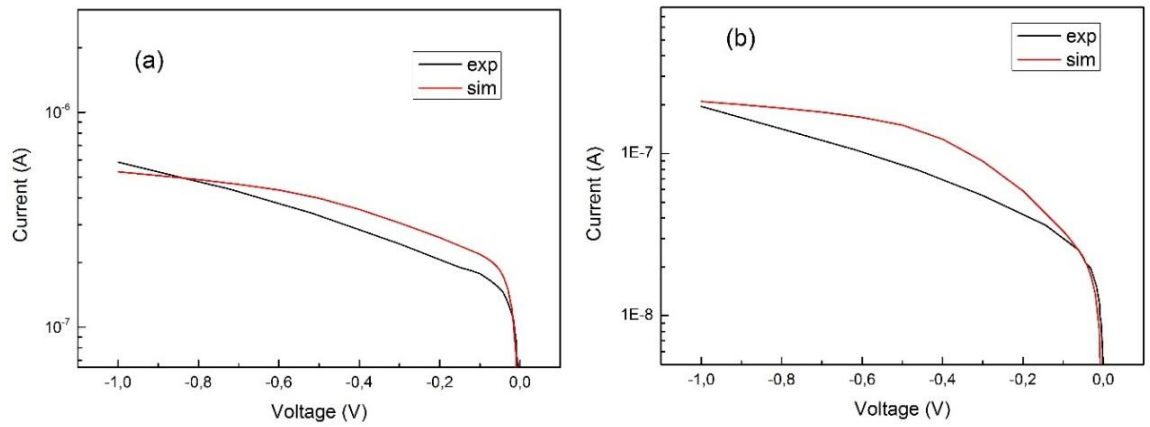


Figure 4.22: Comparison of the simulated I-V characteristics with measurement at: (a) 220 K, (b) 200 K.

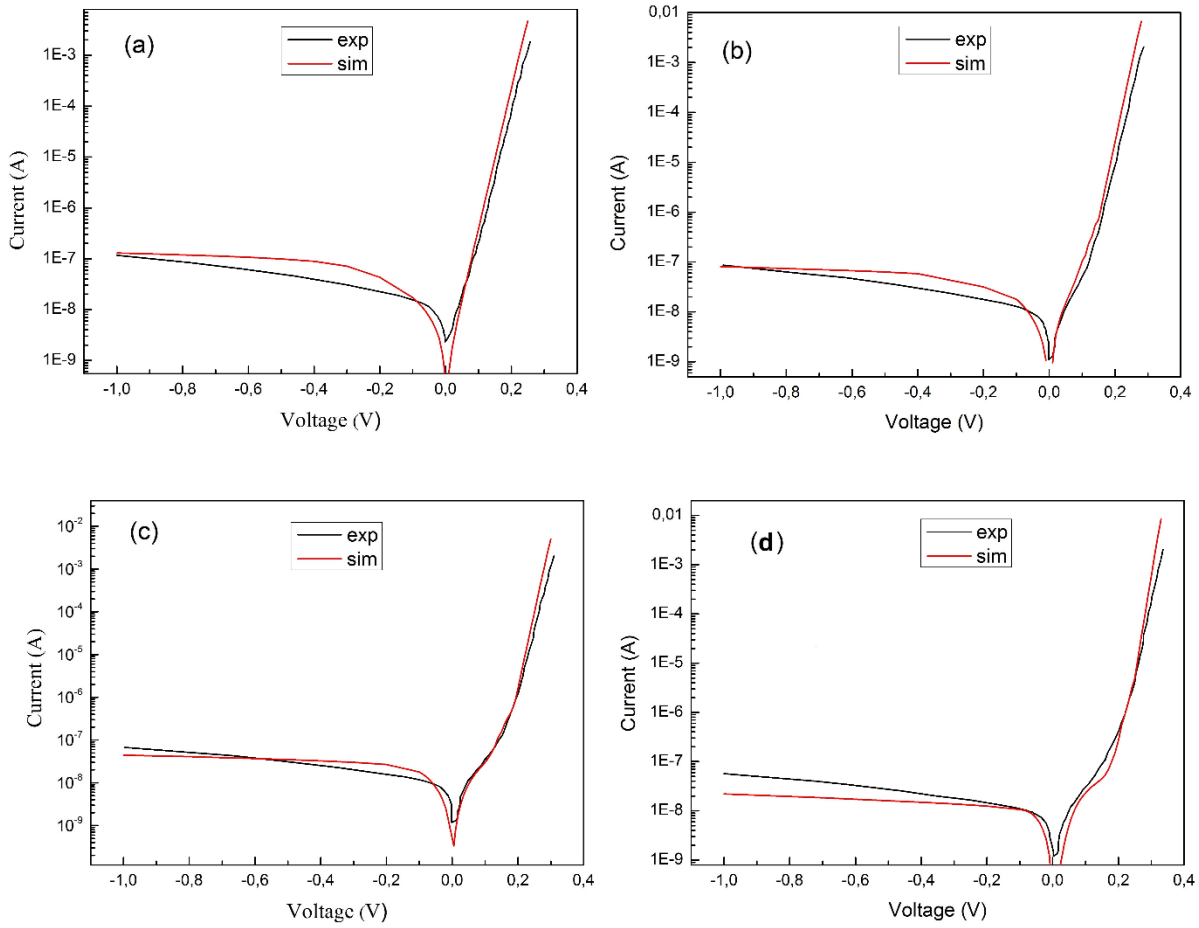


Figure 4.23: Comparison of the simulated I-V characteristics with measurement at: (a) 180 K, (b) 160 K, (c) 140, (d) 120 K.

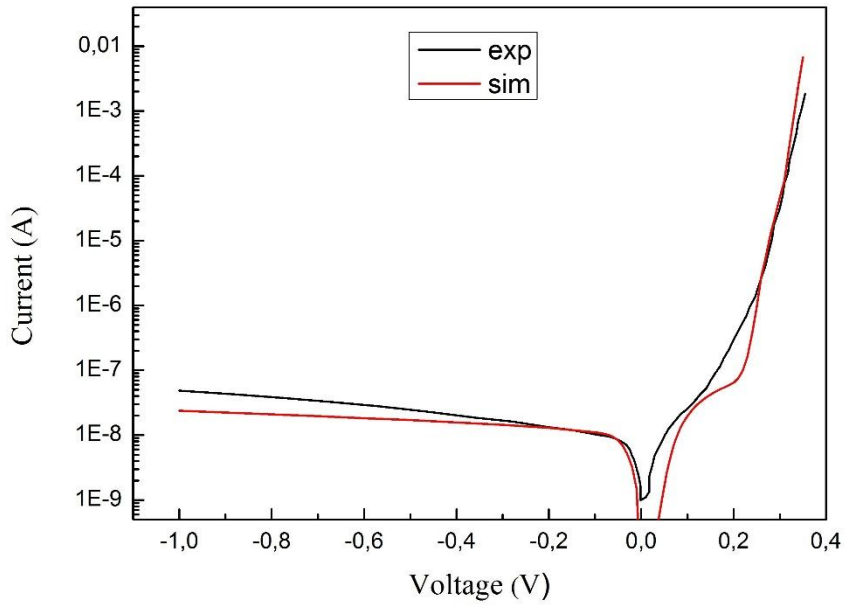


Figure 4.24: Comparison of the simulated I-V characteristics with measurement at 100 K.

4.3.4 Parameters extraction:

As in the high temperature case, n and $\emptyset_{b0}$ were extracted using the standard method, Chueng method (Figure 4.25) and Norde method (figure 4.26), while the series resistance was extracted using the standard and Chueng methods (figure 4.27) and the values are listed in table (4.5). The extracted ideality factor and barrier height values with Chueng and the standard method are almost temperature independent and in close agreement except in 100 K were the extracted parameters with the standard method are temperature dependent. As seen, the standard method and Chueng methods cannot detect Schottky barrier inhomogeneities on the other hand Norde method can detect Schottky inhomogeneities.

As can be seen in figure (4.26) the F(V) plot of Norde function shows two minima, the first minima is in the effective patch bias range (low bias) in the temperature range 140-100 K and the second minima is in the homogeneous barrier bias range (high bias) in all the low temperature range. The values of $\emptyset_{b0}$ extracted with Norde method from the high bias is in good agreement with Chueng an standard method, while the $\emptyset_{b0}$ values extracted from the low bias range are the lowest and shows a strong temperature dependence.

Table 4.5: The extracted n and $\emptyset_{b0}$ values of the real diode with different methods in temperature range 180-100 K.

Temp (K)	n		$\emptyset_{b0}\ (eV)$			
	standard	Cheung	standard	Cheung	Norde	
					Low bias	High bias
180	1.03	1.01	0.447	0.449	/	0.452
160	1.03	1.01	0.444	0.448	/	0.451
140	1.04	1.01	0.441	0.447	0.334	0.451
120	1.04	1.01	0.439	0.445	0.309	0.450
100	1.13	1.01	0.410	0.444	0.277	0.447

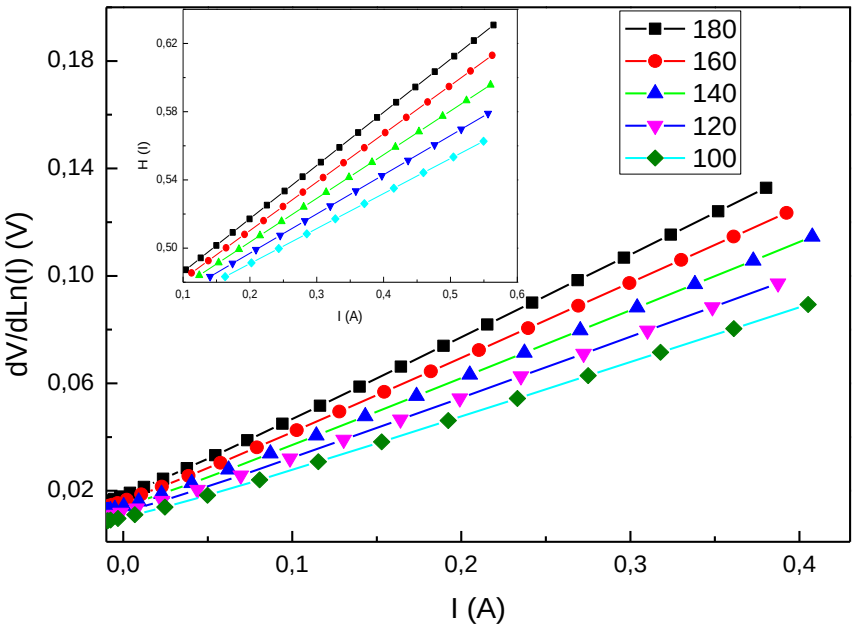


Figure 4.25: The plot of dV/d(LnI) versus I (insert Figureure: plot of H(I) versus I) of the real diode in the temperature range 180-100 K.

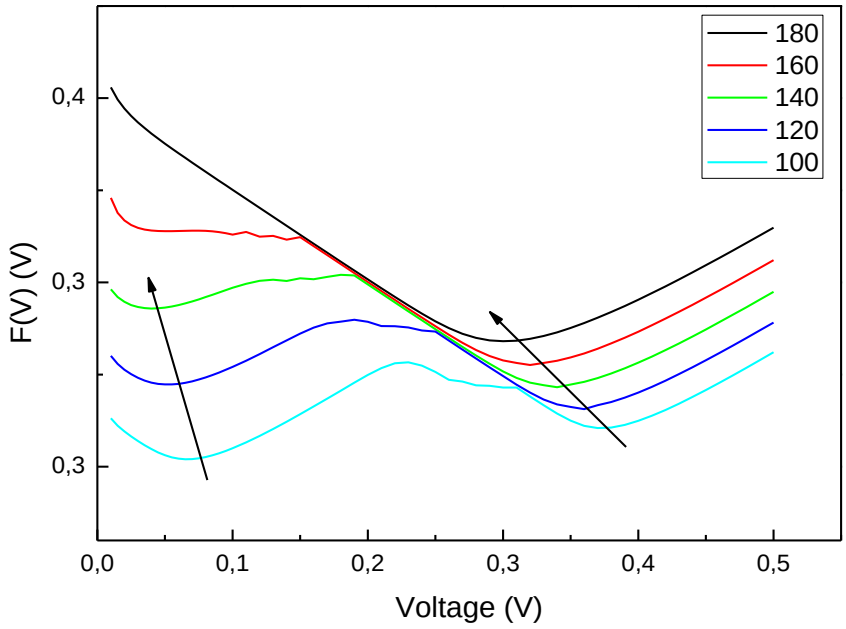


Figure 4.26: The F(V) versus V plot of the real diode in the temperature range 180-100.

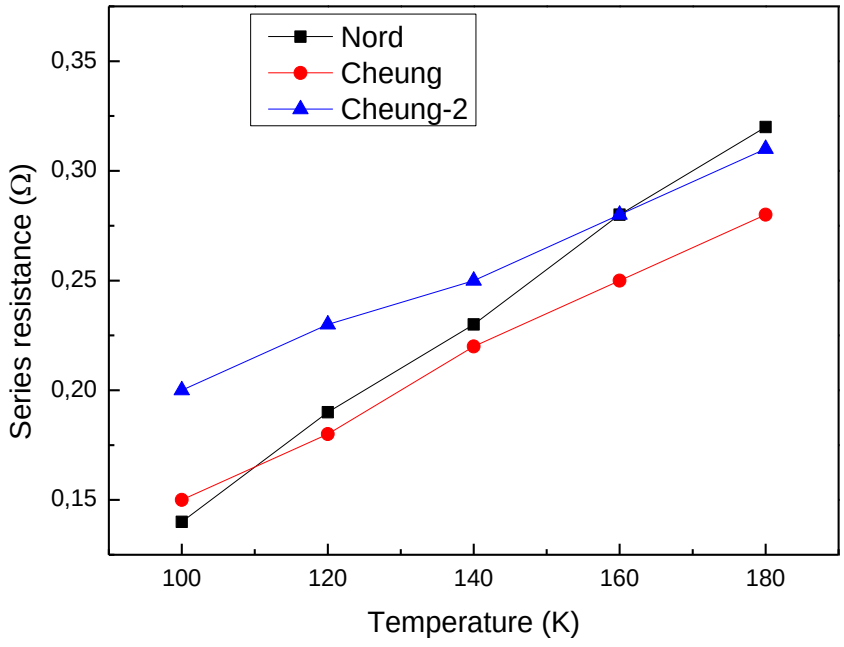


Figure 4.27: The series resistance of the real diode calculated with various methods in the temperature range 180-100 K

4.3 C-V-T characteristics

4.3.1 Near ideal diode:

The simulation is carried out using the same structure and physical models used in the simulation of I-V-T characteristics of the near ideal diode. The frequency of the small signal characteristic used is 1 MHz.

a. Temperature effect

Figure (4.28) displays the simulated reverse bias C^{-2}-V plot of the near ideal diode over the temperature range 100-300 K. The capacitance behavior with revers bias and temperature is ideal, the increase of reverse bias and the decrease of temperature moves the Fermi-level down and up respectively, which increase the depletion width and consequently increase the total positive charge of the ionized donor atoms. As a result, the inverse of capacitance increases with increasing reverse bias and decreasing temperature respectively.

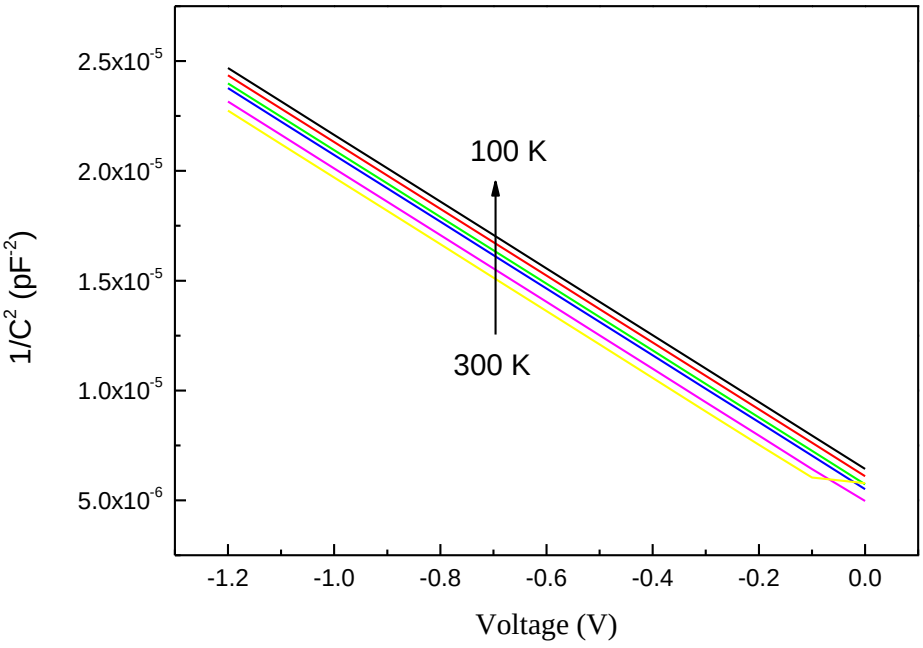


Figure 4.28: The simulated $1/C^2$-V characteristics of the near ideal diode in the temperature range 300-100 K.

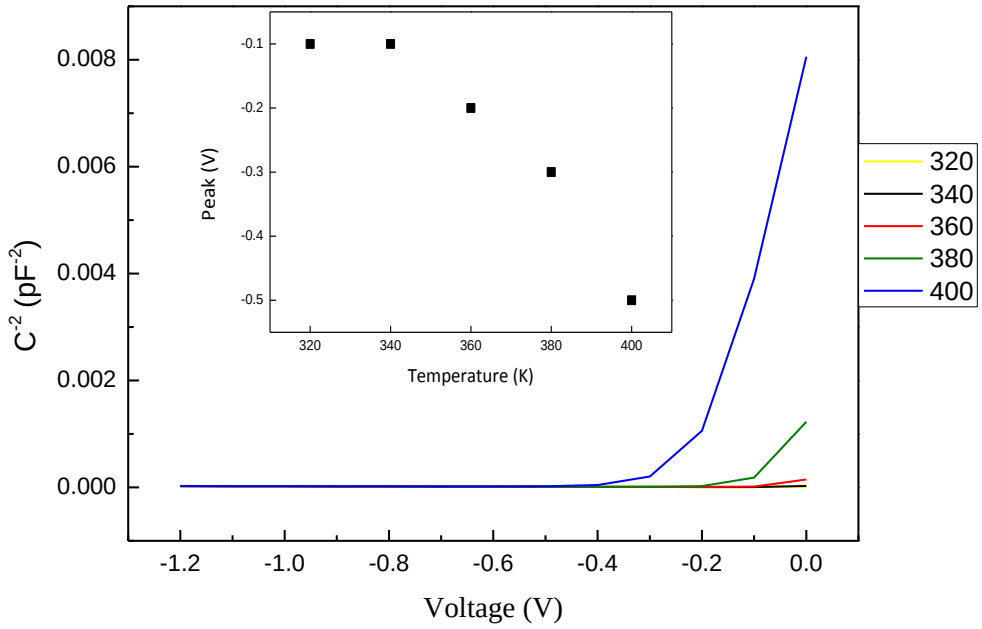


Figure 4.29: The simulated $1/C^2$-V characteristics of the near ideal diode in the temperature range 400-320 K

When the temperature increase above 300 K the invers of capacitance starts to increase with increasing temperature. Also the values of the capacitance shows a minima (peak in the C-V plot), the peak shifting to the reverse bias direction and their values decrease with the increase of the temperature. The shifting of the peak and the increase of the invers capacitance prevents the extraction of the barrier.

b. Barrier height extraction

Using capacitance voltage method discussed in chapter 3, the values of the BH were extracted and listed in table (4.6). The values are constant and equal to the theoretical value. The little difference between $\emptyset_{b0}$ and $\emptyset_{CV}$ attributed almost to image force lowering. Which affect the $\emptyset_{b0}$ and does not affect the $\emptyset_{CV}$, because the CV method is an extrapolation to zero electrical field [78].

Table 4.6: The simulated Φ_{CV} values of the near real diode

Temp (K)	Φ_{CV} (eV)
100	0.435
140	0.424
180	0.419
220	0.423
260	0.424
300	0.426

As can be seen, the ($\emptyset_{CV}$) does not depend on temperature, also C-V characteristics are far away from the experimental ones. Therefore, other phenomena should be considered in the next section.

4.3.2. Real diode

Here we will use the same physical models and the same structure of the real diode used to simulate the I-V-T characteristics, which includes a native oxide with thickness equal to 5 Å and 6×10^{11} cm^{-2} positive interface charge. The frequency of the small signal characteristic used is 1 MHz.

a. Native oxide effect

Figure (4.30) represents the simulated C^{-2}-V plot of the real diode as a function of temperature. We observe the absence of the capacitance peak, except in the temperatures 380 and 400 K. The position of the peak in this two temperatures was shift to the forward bias direction with a few hundred mV, and the value of the peak was reduced compared to the capacitance of the near ideal diode, this behavior attributed to the thin insulator layer at the interface.

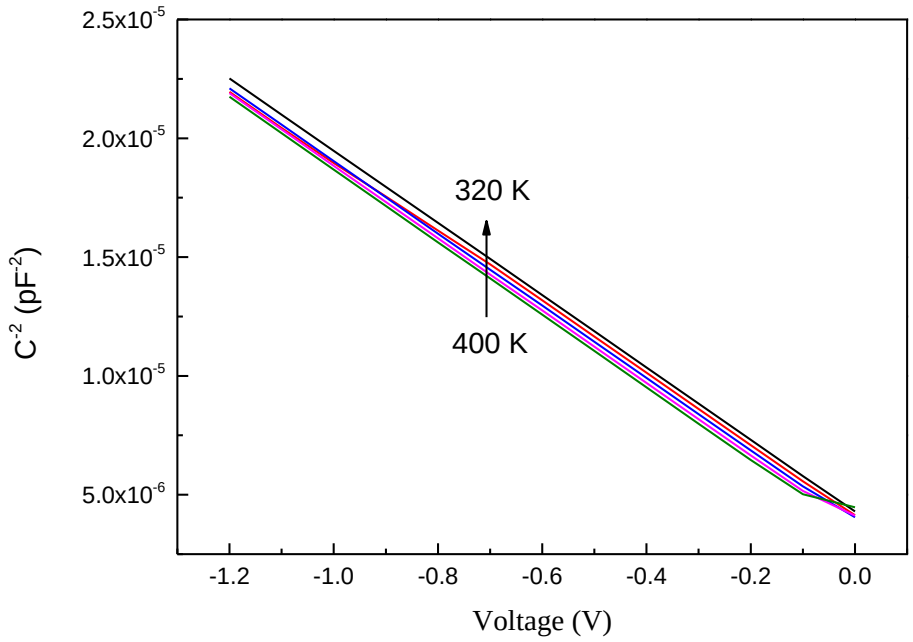


Figure 4.30: Effect of native oxide on the capacitance at high temperature

b. C-V-T characteristics

We saw in the section 4.3.1.a, that the values of the simulated reverse bias C^{-2}-V characteristics of the near ideal diode (figure 4.28) are lower than the experimental ones in the comparison temperature range. And we know from equation (1.20) that the C^{-2} depends on $1/N_i$, that means that the decrease of N_i makes C^{-2} increases. This can be done by the presence of a deep acceptor traps (negatively charged when full) in the depletion region [29], this causes a net decrease in the depletion region charge density and consequently an increase in the values of C^{-2}.

We studied the effect of several traps mentioned by works made spectroscopy measurements on Au/n-InP samples [88-90]. By changing the density and the location of each combination of traps, finally we found four acceptor traps that give the same values and especially the same slope of the experimental C^{-2}-V characteristics in the temperature range 100-300 K. The traps are, E1 (Ec-0.69), E2 (Ec-0.62), E3 (Ec-0.51) and E4 (Ec-0.43) with a density close to 10% of the doping concentration.

Figure (4.31) represents simulated C^{-2}-V plot of the real diode in the temperature range 100-300 K by step of 40 K.

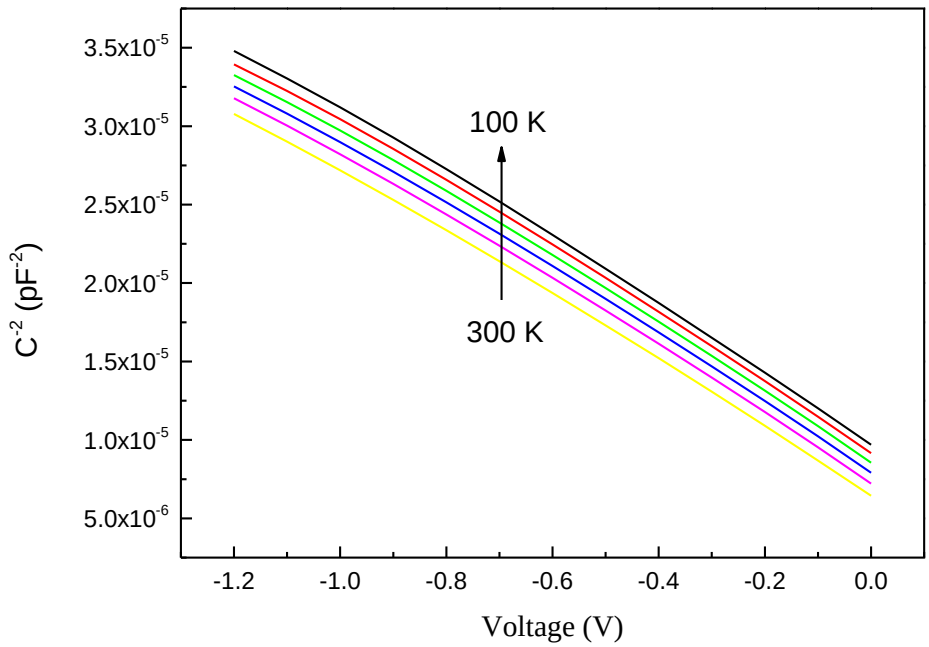


Figure 4.31: The simulated $1/C^2$-V characteristics of the real diode in the temperature range 100-300 K.

The C^{-2} values of the real diode are in very good agreement with experimental data, this is a strong evidence that proves the presence of the previous traps (E1, E2, E3 and E4) in the experimental sample. A detailed comparison with the experimental data in each temperature in the range 300-100 K is shown in figure (4.32).

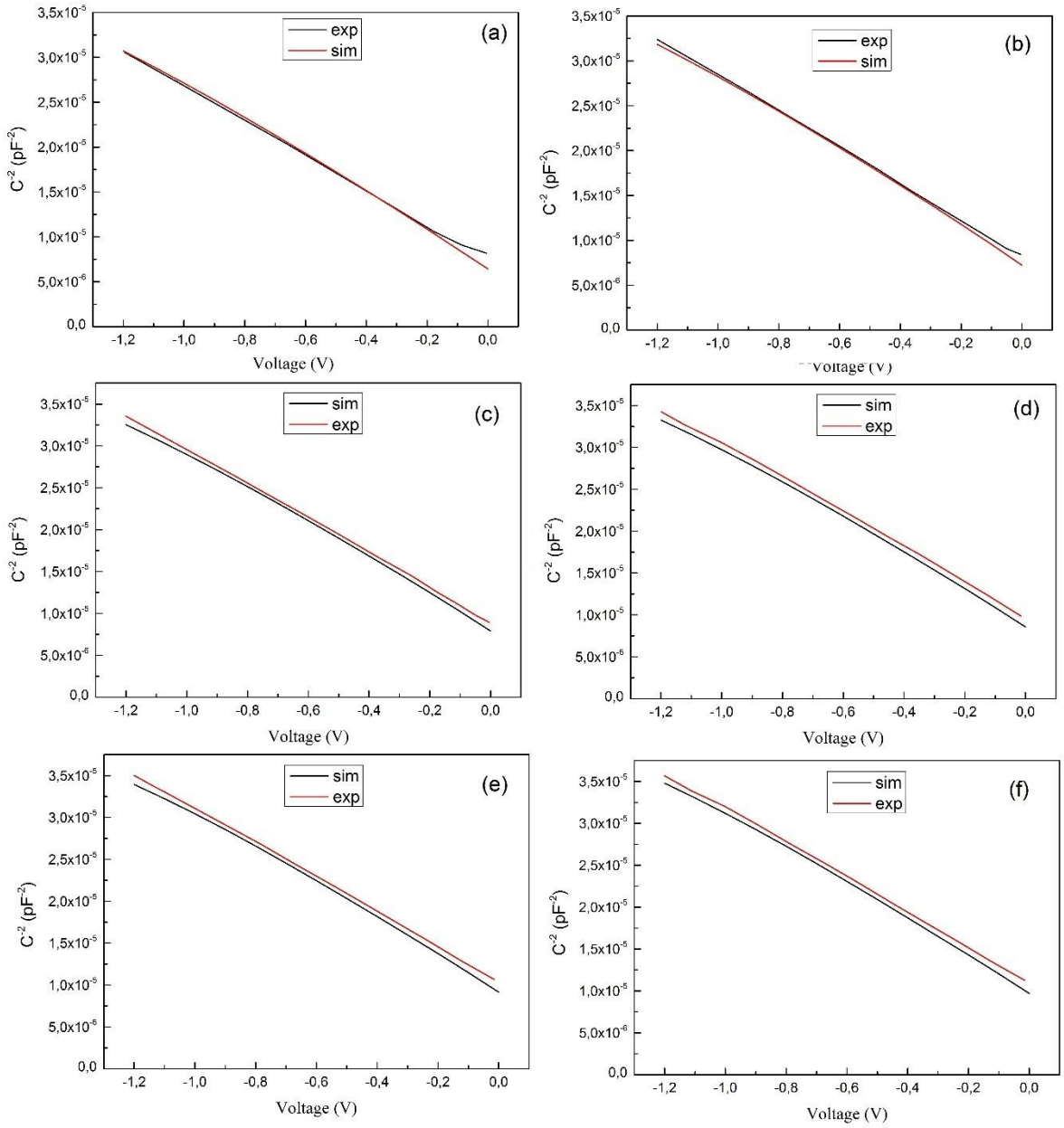


Figure 4.32: Comparison of the simulated C-V characteristics with measurement at: (a) 300 K, (b) 260 K, (c) 220, (d) 180, (e) 140, (f) 100 K.

c. Barrier height extraction

As listed in table (4.7), Φ_{CV} increases with decreasing temperature, this temperature dependence of Φ_{CV} is attributed to the deep acceptor in the depletion region. The ionized acceptor traps below the Fermi level decrease the capacitance making the built-in voltage increases and consequently the increase of the BH. In more details, the major role of the Φ_{CV} temperature

dependence is the level E4, due to the dependence of its ionization on bias and temperature. Because the low activation energy of this level, its ionization density decreases with the increasing of reverse bias, which consequently raise the built-in voltage. When the temperature decreases the Fermi level move up, which increases the ionization density of the level E4 compared to the previous temperature in the same reverse bias, which increases the built-in voltage compared to the previous temperature.

Table 4.7: The simulated Φ_{CV} values of the real diode with experimental ones.

Temp (K)	Φ_{CV} (eV)	
	Simul	Exp (ref.85)
100	0.549	0.547
140	0.554	0.543
180	0.540	0.539
220	0.527	0.527
260	0.515	0.517
300	0.506	0.508

As can be seen in table (4.7), the BH values from C-V characteristics ($\emptyset_{CV}$) is larger than those from I-V characteristics ($\emptyset_{b0}$) in the temperature range 200-300 K. This difference is larger than the image force lowering values, on contrary to the case of the near ideal diode.

4.4. The discrepancy between the barrier height extracted from C-V and I-V characteristics

Based on the previous results obtained from I-V-T and C-V-T characteristics, we can explain the discrepancy between $\emptyset_{CV}$ and $\emptyset_{b0}$. If the barrier at the MS interface is homogeneous and thermionic current is the dominant conduction mechanism and there is no deep traps in the depletion region of the semiconductor. In this case, the values of $\emptyset_{CV}$ and $\emptyset_{b0}$ will be equal, if we neglect the image force lowering. However, when there is an interfacial layer at the MS interface, the tunneling current dominates the transport mechanism, which causes the temperature dependence of the $\emptyset_{b0}$, while the $\emptyset_{CV}$ is insensitive to tunneling current. On the other hand, the presence of deep traps in the depletion region of the semiconductor causes the temperature dependence of the $\emptyset_{CV}$, while the $\emptyset_{b0}$ is insensitive to the traps, because the low density traps do not affect the forward current.

4.5 Neutral region trap effect on the series resistance

The series resistance of Schottky diode has been studied for a long time as important parameters that affect the I-V characteristics likewise the other parameters, while those studies did not give a convincing interpretation of the physical phenomenon that causes the series resistance effect. The only interpretations seen are the semiconductor and contact resistivity, while these two interpretations are found incorrect by our simulation since we have studied the effect of these two parameters. Since the series resistance is known as the voltage drop across the quasi natural region, the effect of deep trap should be considered.

Here we will use the same deep tarp used in the simulation of the C-V-T characteristics with density equal to 10 % of the diode concentration to simulate the I-V characteristics of the real diode in 300 K and then extract the series resistance. The trap depth will be varied from 0.5 μm (almost close to the depletion region width) to 3.5 μm.

As seen in figure (4.33) the current of the simulated I-V characteristic with 3.5 μm of trap depth was reduced in the series resistance region compared to the current of the simulated I-V characteristic with 0.5 μm of trap depth, while the current in the reverse and low forward bias did not affected. This is because in the forward bias above the built-in voltage, the electrical field created due to the ionized acceptor in the neutral region in opposite to the junction electrical field becomes greater than the junction electrical field itself, which makes the electrons recombine with the deep trap acceptor in the neutral region. The information of the electrical filed and recombination rate were extracted from the structure files of diodes with 0.5 and 3.5 μm of traps depth in several bias conditions.

The series resistance of the two I-V curves shown in figure (4.33) was calculated using Norde method. As can be seen in figure (4.34), the series resistance of the I-V curve simulated with 3.5 μm of trap depth found to be greater by 5 times than this of I-V curve simulated with 0.5 μm of trap depth.

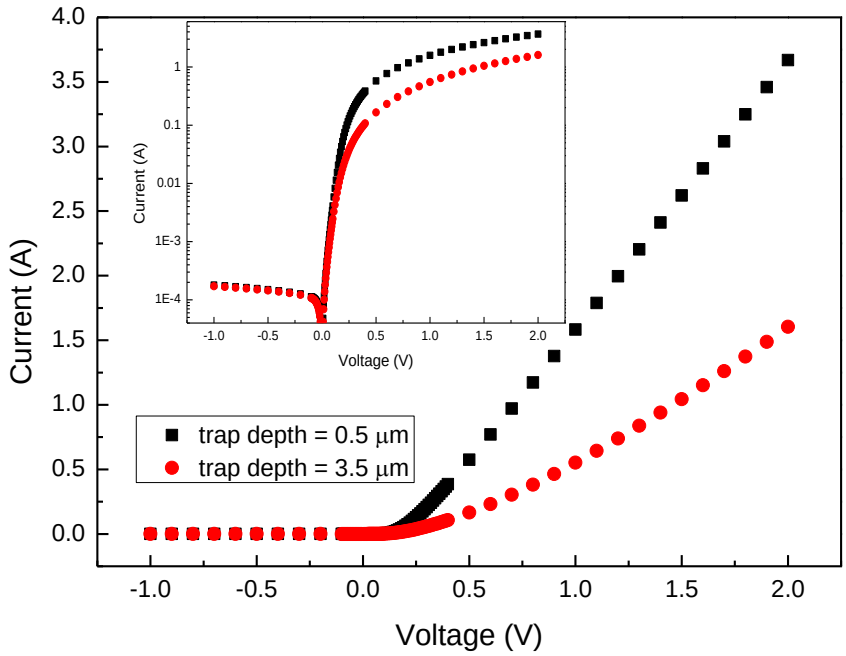


Figure 4.33: The I-V characteristic of the real diode with different trap depth at 300 K in linear scale (the insert in semi-logarithmic scale).

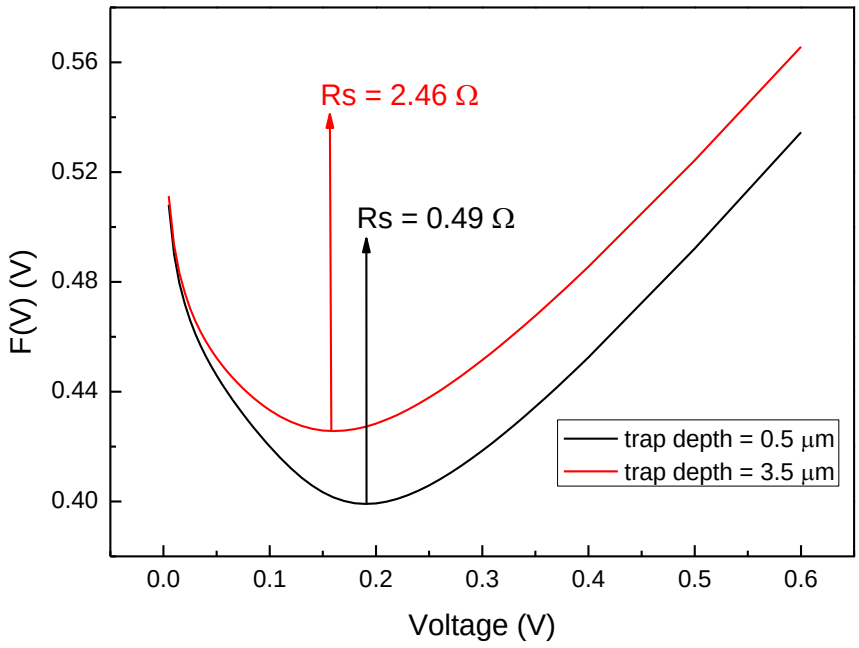


Figure 4.34: The F(V) versus V plot of the I-V characteristic in figure (4.31).

4.6 I-V-T characteristics intersection:

The intersection of forward I-V characteristics measured at various temperature is often observed in Schottky diodes data at different bias range. Subhash Chand in [91] has illustrated analytically that the intersection of I-V curves is an inherent property of any Schottky diodes and is normally hidden due to saturation in current caused by series resistance, this means that the series resistance has an important effect on the I-V characteristics intersection. This assumption is supported by several experimental results, for example the measured I-V characteristics by Tascıoglu et all [92] shows an intersection in 1.4 V with a series resistance equal to 334.2 Ω in 320 K. In the same context the results of Karatas et all [19] shows an intersection in 0.9 V with a series resistance equal to 50.1 Ω, also the I-V curves of Karatas et all [19] intersects in 0.85 V with a series resistance equal to 40.6 Ω in 300 K.

In our case the I-V intersection was found in 0.49 V for the near ideal diode, real diode and the homogeneous diode, this is probably due to the convergence of the series resistance values of these diodes, that is the series resistance values difference must be significant to affect the intersection point of the I-V curves.

Here will study the effect of the series resistance on the I-V curves intersection by simulating the I-V characteristics of the real diode in two temperatures (300 and 200 K) using two values of the series resistance (0.49 Ω and 2.46 Ω). The previous values of the series resistance will be used indirectly by using deep traps. In more details, in the previous section the real diode with deep traps that have density equal to 10 % of the diode concentration and two depths (0.5 and 3.5 μm) found to has a series resistance equal to (0.49 and 2.46 Ω) respectively.

The obtained results of the simulated real diodes with series resistance values equal to 0.49 and 2.46 Ω are shown in figure (4.35) and figure (4.36) respectively. As can be seen, the intersection point of the I-V curves with series resistance equal to 0.49 Ω found at 0.49 V on the other hand the intersection point of the I-V curves with series resistance equal to 2.46 Ω found at 0.75 V.

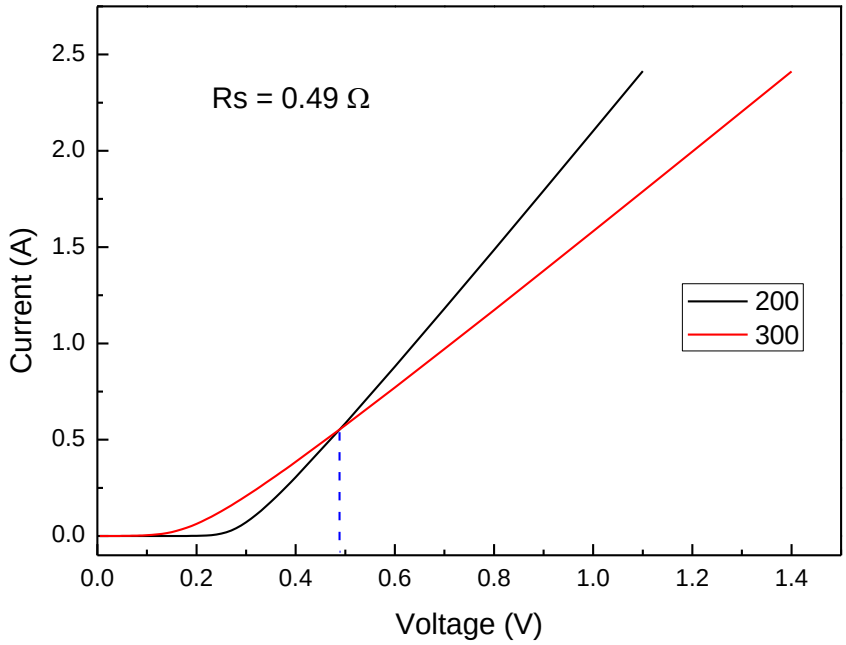


Figure 4.35: The I-V characteristic of the real diode at 300 and 200 K with series resistance values equal to 0.49 Ω.

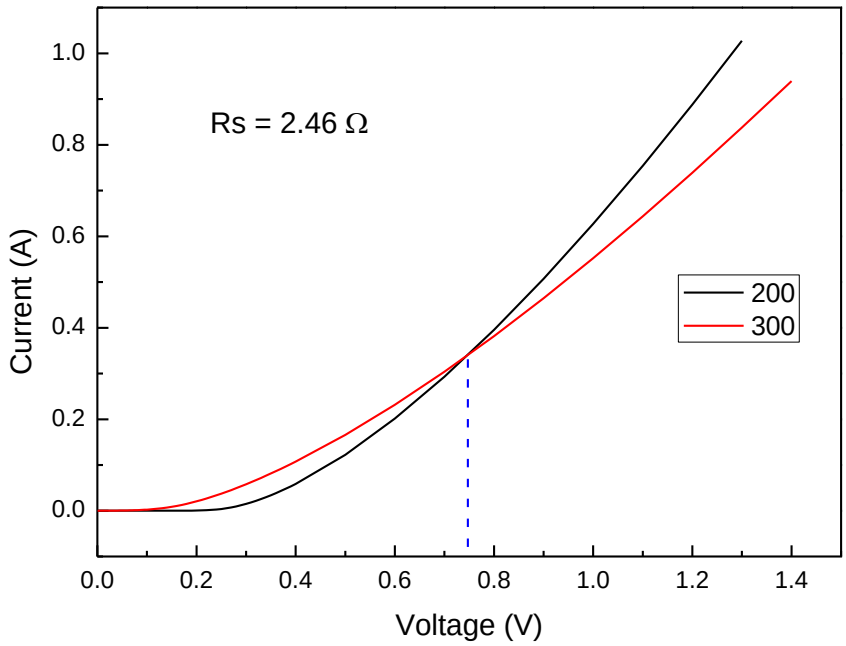


Figure 4.36: The I-V characteristic of the real diode at 300 and 200 K with series resistance values equal to 2.46 Ω.

Conclusion

In conclusion, both current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the Au/n-InP SBD have been simulated with atlas Silvaco-Tcad in the temperature range 400-100 K. Both characteristics were simulated in near ideal and real cases. The near ideal case take in to account the material properties and their temperature dependence, TE current, carrier generation-recombination processes and Schottky effect. The real case including in addition to the previous phenomena interface states, traps and tunneling current. In each case and temperature range the diodes parameters ($\emptyset_{b0}$, n, R_s and $\emptyset_{CV}$) were extracted using different extraction methods.

By analyzing main diode parameters behavior with the change of temperature in the near ideal and real cases, we were able to explain the experimentally observed abnormal temperature dependence of these parameters and the discrepancy between $\emptyset_{b0}$ and $\emptyset_{CV}$.

In the near ideal case, the littleness of the BH and the effect of the temperature found to be the cause of the presence of leakage current above 360 K and a high series resistance compared to the real case. The ideality factor of this diode found to deviate from unity and shows a temperature dependence due to the effect of series resistance.

The presence of thin native oxide layer with 5 Å of thickness at the interface of the diode eliminates TE current because it does not have a sufficient energy to surmount the high potential across the native oxide layer, which makes tunneling current the dominating transport mechanism. In addition the presence of native oxide layer reduce the leakage current and the series resistance.

In the high temperature regime (400-200 K), the deviation of the transport mechanism from TE current found to affect the zero-bias BH in contrary to the ideality factor. This is because tunneling current does not has the same saturation current values of thermionic emission current while it has almost the same slope of TE current.

Also, the results have shown that the linearity of Richardson plot is a consequence of the barrier homogeneities, which mean that the inhomogeneity of the barrier does not affect the transport in the temperature rang where Richardson plot have a linear form.

Concerning the SBH inhomogeneity, the analyses of I-V-T characteristics based on Werner and Guttler model found to be incorrect due to the disadvantage of this model in contrary to Tung model which is more accurate.

The effective patch parameters (the effective area and the BH) of an inhomogeneous SBH extracted from modified Richardson plot with Tung model found to be incorrect because this model is based on TE theory whereas the dominated current in the experimental simple is tunneling current.

The simulation of I-V characteristics in low temperature regime with inhomogeneous BH proved that the low bias forward current in this temperature range 160-100 K is dominated by the electrons flows through an effective patch with radius and BH equal to 0.1 μm and 0.1 eV respectively. On the other hand the reverse current in the temperature range 220-100 K is dominated by the electrons flows through an effective patch with radius equal to 0.02 μm and BH between 0.02 and 0.01 eV. This near zero BH of the reverse bias effective patch whose prevent the reverse current to saturate in the temperature range 220-100 K.

The parameters extraction methods used in this work are in close agreement and gives almost the same parameters values except in case when SBH inhomogeneity affect the transport of current, in this case Norde method is the only method that can detect SBH inhomogeneity.

The near ideal diode capacitance above 300 K shows a peak (minima in the C^{-2}-V plot), the peak shifting to the reverse bias direction and their values decrease with the increase of the temperature. While the extracted BH is equal to the theoretical value and did not shows a temperature dependence.

The peak observed in the near diode capacitance was eliminated in real diode capacitance due to the presence of native oxide layer. In addition, the simulation of the real diode capacitance proves the presence of four deep acceptor traps with density close to 10 % of the diode doping concentration. These deep traps were found to be responsible of the temperature dependence of $\emptyset_{CV}$.

The discrepancy between $\emptyset_{b0}$ and $\emptyset_{CV}$ in the simulated temperature range can clearly be explained by the difference of the temperature dependence causes, that is, the $\emptyset_{b0}$ temperature dependence is due to the deviation from TE current, and the $\emptyset_{CV}$ temperature dependence is due to the deep acceptor traps.

Moreover, the deep traps acceptor has a significant effect on the series resistance, that is, as the series resistance increase as the trap depth in the neutral region increase.

Finely, the intersection point of the I-V-T characteristics found to depend on the series resistance value. That is, as the series resistance increase as the I-V-T intersection point shift in the forward bias direction.

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