Pergamon

0038-1101(94)00249-5

Solid-State Electronics Vol. 38, No. 7, pp. 1413–1421, 1995

0038-1101/95 $9.50 + 0.00

BACKGATING EFFECTS IN GaAs FETs WITH A CHANNEL-SEMI-INSULATING SUBSTRATE BOUNDARY

N. SENGOUGA[1] and B. K. JONES[2]†

[1]Institut d'Electrotechnique, Centre Universitaire de Biskra, 07000 Biskra, Algeria and [2]School of Physics and Chemistry, Lancaster University, Lancaster LA1 4YB, England

(Received 24 January 1993; in revised form 4 November 1994)

Abstract—Several methods are presented to relate the backgating effects to hole traps near the channel–semi-insulating substrate interface of GaAs MESFETs. By analysis of the variation of the individual properties of the device the time dependence of backgating is shown to be related to the time constants of these traps and the temperature dependence of backgating is related to the temperature dependence of the emission from these traps. The current between the semi-insulating substrate and the channel is shown to be dominated by a generation mechanism rather than the Trap Fill Limited model. This means that a space charge region exists at the channel–substrate interface and the properties can be approximated to an n–p^- junction.

1. INTRODUCTION

The reduction of the GaAs field effect transistor (GaAs FET) channel conductance by a negative voltage applied to the semi-insulating (SI) substrate is termed backgating or sidegating[1,2]. Earlier studies have related this phenomenon to the formation of a space charge region (SCR) at the channel–substrate interface[3]. Later investigations have shown that backgating is also related to the substrate conduction[4,5]. The argument was that a threshold for the channel conduction reduction was observed and is exactly the same as the voltage at which the substrate current changes from being ohmic to space charge limited. However some recent studies disputed this relation and suggested that backgating is related to impact ionisation[6]. However, in other studies no threshold was observed for backgating[7,8] and therefore the threshold is not a definite criterion for backgating.

There are so many effects related to backgating that it is considered the most serious problem in discrete devices as well as integrated circuits[9,10]. For example the C–V characteristics of a GaAs FET can be affected by backgating[3]. Most of the low frequency anomalies[11], light-induced effects[12], low frequency oscillations and g–r noise[13–15] and most of the drift phenomena[16] are related to the traps, near the channel–substrate interface, which also cause backgating[17].

A lot of effort has been devoted to the elimination of backgating or at least reducing it. In the early days, a high purity epitaxially grown buffer layer achieved some success in reducing backgating[7,18,19]. However this buffer layer did not eliminate the problem as it may itself contain deep traps[20]. Backgating was also reported to be reduced by proton[21] and oxygen[22] implantation in the SI substrate. A p-type layer buried under the channel also reduced backgating and improved the device characteristics[23], but it seems that the most effective way, up to now, to reduce the backgating related effects is the growth of a buffer layer by MBE at low substrate temperatures[24,25].

This paper is one of a series by the Lancaster group which discusses the properties and methods of analysis of trap effects in GaAs FETs using a wide variety of techniques. It will be shown by studying the substrate conduction that backgating in these samples is the result of the formation of a space charge region (SCR) at the channel–substrate interface. It will also be shown that hole traps near the channel–substrate interface are responsible for the formation of this SCR by relating the time and temperature dependence of backgating to the time constants and thermal emission of these hole traps observed by DLTS. The density of these traps is also measured. The analysis is of direct relevance to other n-GaAs-semi-insulating junctions.

2. EXPERIMENTS

The specimens used are low noise GaAs FETs type P35-1105 batch F2137, made by Plessey 3-5. The device has a recessed gate structure using doped epitaxial GaAs grown on a mesa on Cr-doped HB semi-insulating GaAs with a buffer layer. The buffer layer is $\sim 0.85\,\mu$m thick and the gate is $\sim 0.8\,\mu$m

†To whom all correspondence should be addressed.

long. The substrate contact is on the reverse side of the substrate and is nominally ohmic. They are not typical of current commercial devices.

The specimens were first characterised by DLTS in the ohmic channel conductance following a voltage step applied to the substrate. In the DLTS spectrum two dominant hole-like traps labelled H_1 and H_0 were observed[26,27]. They have a time constant of 100 ms at 318 and 365 K, respectively.

Three sets of experiments were performed to investigate the backgating phenomenon.

2.1. Time dependence of backgating

The time dependence of a backgating experiment is based on that of Jin and Jones[28] with some modifications. In the original method, the time dependence of the device characteristics, G_{DS} (measured at small V_{DS}), due to trap emptying or filling after a voltage step is applied to the gate, are studied. At various times during this transient rapid $I_{DS}(V_{GS})$ characteristics are taken and the device parameters (the pinch-off voltage V_P, the full open channel resistance R_{CO} and the parasitic series resistance R_S) are then evaluated using the Fukui procedure which will be described later.

This gives the magnitude and time constant of the changes in these parameters due to the traps, and hence their number and location. In the present method, instead of studying the time effect on the $I_{DS}(V_{GS})$ characteristics after an exciting pulse on the gate, this effect is studied after an exciting pulse on the substrate. The device is held at a fixed temperature of interest, a bias of $V_{BS} = -10$ V is then applied to the substrate using a pulse generator for a period $t = W_T$ before the $I_{DS}(V_{GS})$ characteristics are measured rapidly using another pulse generator. The pulses on the gate and the substrate are shown in Fig. 1. This experiment is repeated, at the same temperature, for several values of W_T. This procedure was suggested by Jin[29].

2.2. Temperature dependence of backgating

The temperature dependence of backgating is studied by measuring the transconductance $I_{DS}(V_{GS})$ characteristics with the substrate voltage V_{BS} as a parameter at different temperatures. I_{DS} is measured using a Solartron 7150 multimeter and V_{GS} is applied using a D/A converter and is varied by a computer programme. One very important factor in this experiment beside the temperature is the experimental time constant. This importance arises from the expectation that backgating is the result of thermally activated emission from traps in the substrate or near the channel–substrate interface. In this experiment we distinguish between two experimental time constants, the gate time constant and the substrate time constant. The gate time constant is the time required to measure the transconductance $I_{DS}(V_{GS})$ characteristics at constant temperature and substrate voltage. This is ~ 40 s. The substrate time constant is the duration of applying V_{BS} before the transconductance $I_{DS}(V_{GS})$ characteristics are measured. This is ~ 120 s. In this experiment the gate time constant is not important because, for different substrate biases, this time is the same. Therefore any change in the device characteristics between two substrate biases, for example, is only due to the change in the substrate bias conditions and has no relation with the gate bias conditions.

2.3. Substrate conduction

The substrate current I_{BS} is measured simultaneously with the drain–source current I_{DS} as a function of the substrate voltage V_{BS} in the ohmic region of the device characteristics ($V_{DS} = 0.1$ V). The substrate current is measured as a voltage drop across a 1 MΩ resistor in series with the substrate. The gate voltage was kept at $V_{GS} = 0$ V. Since it is expected that traps will play a major role in this experiment it is necessary to mention briefly the experimental time constant. The sampling time is at least 5 s but not more than 10 s. These measurements were repeated at different temperatures ranging from 127 to 388 K.

3. RESULTS AND DISCUSSION

3.1. Time dependence of backgating

The $I_{DS}(V_{GS})$ characteristics were measured with W_T as a parameter and $V_{BS} = -10$ V and converted to $G_{DS}(V_{GS})$. The results are shown, at two different temperatures corresponding to the traps H_1 and H_0, in Fig. 2. The results were analysed to identify which of the device parameters (V_P, R_{CO}, R_S) are most affected by backgating (or emission from the two traps). The analysis also yields the time dependence of these parameters which will be compared with the time constants of the traps observed by DLTS. For this purpose the Fukui procedure was used[30]. This procedure makes use of the relation between the

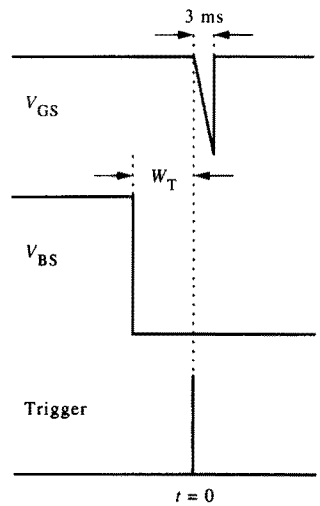

Fig. 1. Timing diagrams for gate and substrate pulsing and triggering.

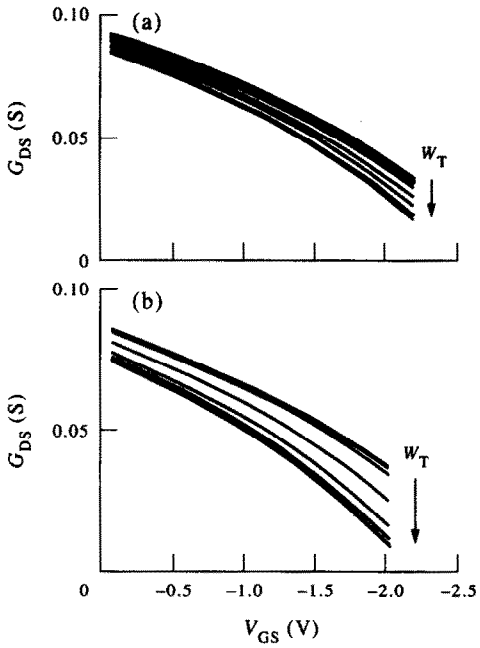

Fig. 2. The $G_{DS}(V_{GS})$ characteristics for the device F2137/10, (a) at $T = 318$ K (trap: H_1) and (b) at $T = 370$ K (trap: H_0) with the delay time W_T as a parameter and $V_{BS} = -10$ V.

channel resistance R_{DS} and the channel opening factor w. The total channel resistance is given by:

$$R_{DS} = R_C + R_S, \tag{1}$$

where R_{DS} is given, as a function of the measured G_{DS}, by:

$$R_{DS} = \frac{1}{G_{DS}}, \tag{2}$$

and R_C and R_S are the resistances of the gated and ungated channel regions respectively. In this equation it is assumed that the channel has a uniform doping density and only R_C is V_{GS} dependent since the depletion resulting from the application of V_{GS} spreads normal to the channel only so that:

$$\begin{aligned} R_C &= R_{CO}\frac{a_0}{a} \\ &= R_{CO}\left[1 - \sqrt{\frac{V_B - V_{GS}}{V_B + V_P}}\right]^{-1} \\ &= R_{CO}w, \end{aligned} \tag{3}$$

where

$$w = \left[1 - \sqrt{\frac{V_B - V_{GS}}{V_B + V_P}}\right]^{-1} \tag{4}$$

and a_0 is the full open channel width, a is the channel width, V_B is the Schottky barrier built-in voltage, V_P is the pinch-off voltage and w is known as the channel opening factor. Therefore equation (1) becomes:

$$R_{DS} = R_{CO}w + R_S \tag{5}$$

$$= R_{CO}\left[1 - \sqrt{\frac{V_B - V_{GS}}{V_B + V_P}}\right]^{-1} + R_S. \tag{6}$$

So if the plots $I_{DS}(V_{GS})$ are transformed to $R_{DS}(w)$ plots then a straight line should be obtained providing that V_P is correctly selected. V_B is assumed to be 0.75 V. The selection of V_P to obtain a straight line plot of $R_{DS}(w)$ is achieved by minimising the sum of the squares of the difference between the experimental data and the fitted function for several values of V_P (least square method). Once the best fit V_P is selected to obtain a straight line plot of $R_{DS}(w)$, R_{CO} can be calculated as the slope of this straight line and R_S as its intersection with the R_{DS} axis. To avoid any errors which may affect the fitting quality, data near the Debye tail and the pinch-off regions are not included in the fitting. Examples of the $R_{DS}(w)$ plots with W_T as a parameter are shown in Fig. 3. The percentage change in the device parameters evaluated from these fittings are shown in Fig. 4 as a function of the delay time W_T. In these figures are also shown (in solid lines) the time fittings of the device parameters change during the transient assuming that these parameters depend on time as $\exp(-W_T/\tau)$. The time constants fitted are shown with each curve. Let us now discuss the meaning of these results.

First, as the delay time W_T increase, V_P decreases while both R_{CO} and R_S increase. This can only be explained by a decrease in the full open channel width a_0 since $V_P \propto a_0^2$ while $R_{CO} \propto a_0^{-1}$ and $R_S \propto (a_r + a_0)^{-1}$ where a_r is the recessed region depth. The decrease in a_0 is due to the spread of a depletion region from the back interface following a negative voltage applied to the substrate. As W_T increases the

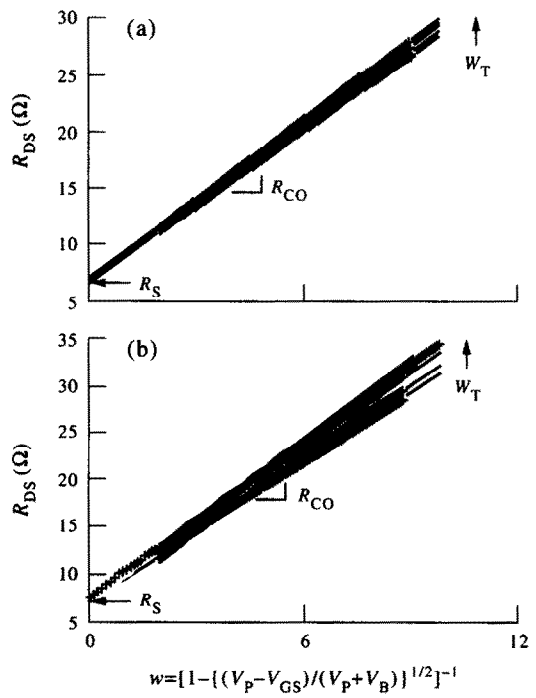

Fig. 3. Transformation of the $G_{DS}(V_{GS})$ characteristics of Fig. 2 to $R_{DS}(w)$ plots (symbols = experimental data; solid lines = fittings) using the best fitted V_P for different values of W_T for H_1 (a) and H_0 (b).

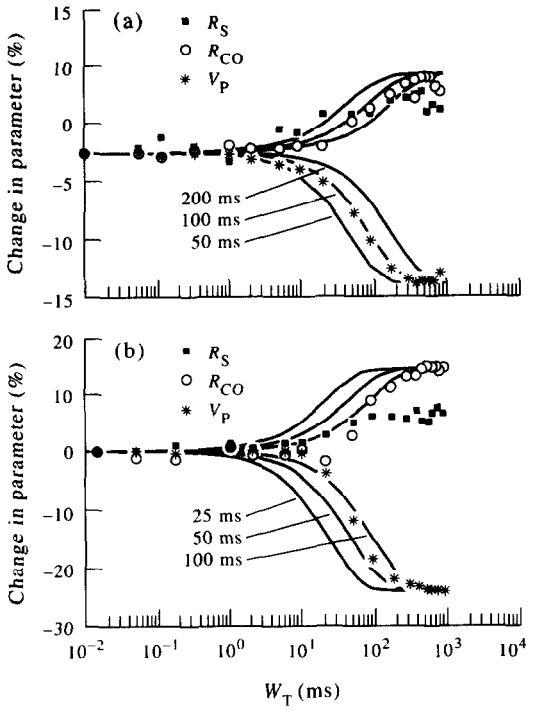

Fig. 4. The device parameters fitted/calculated from the fitting in Fig. 3 (symbols) and the time fitting (solid lines) to compare with the time constants of H_1 (a) and H_0 (b).

hole-like traps (H_1 and H_0) are given more time to emit holes, which means more ionised traps, leaving an excess negative charge in the substrate side of the channel–substrate interface. This negative charge must be neutralised by a positive charge in the channel side. This is achieved at the expense of creating a depletion region in the channel, hence a reduction in its effective width leading to the observed conduction reduction by the negative substrate voltage. Second, the characteristic time constant fitted to the time dependence of the device parameters, as shown in Fig. 4, is very comparable to the substrate DLTS time constants of H_1 and H_0, ~100 and 50 ms respectively.

3.2. *Temperature dependence of backgating*

A voltage of $V_{DS} = 0.1$ V is applied to the drain, then the transconductance $I_{DS}(V_{GS})$ characteristics are measured with the substrate voltage V_{BS} as a parameter. The substrate voltages used are: 0, −5, −10, −20 and −35 V. This experiment is repeated at 16 temperatures ranging from 127 to 408 K. Examples of results of this experiment are shown in Fig. 5. Before analysing the results in detail some preliminary observations are outlined. At low temperature (127 K for example), no backgating effect is observed. This is because at this temperature the time constant of the fastest of any of the traps is nowhere near the experimental time constant. Simple calculations, assuming that the traps capture cross-section σ is independent of temperature show that τ(for H_1 at 127 K) $\approx 6 \times 10^{17}$ s. Therefore no trap is able to respond to the bias changes. As the temperature increases there is still no observed backgating until it reaches ~240 K. At this temperature the effect of backgating begins to manifest itself. The calculated time constant at this temperature is ~14 min. The effect increases with increasing temperature all the way except at ~290–300 K where it is slightly reduced. This is because of the appearance of a small (in size) electron-like trap (EL2)[31]. Then the effect increases again until it reaches some sort of saturation above 400 K.

Now these characteristics are analysed in more detail. In this analysis, the Fukui procedure presented above is used to fit the experimental data to characterise which of the device parameters (V_P, R_{CO} and R_S) are most affected by backgating. The $R_{DS}(w)$ plots at $T = 408$ K with V_{BS} as a parameter are shown in Fig. 6. The device parameters fitted/calculated are shown in Fig. 7. Now the effect of V_{BS} on V_P, R_{CO} and R_S is discussed. First let us call the curves corresponding to $V_{BS} = 0$, −5, −10, −20 and −35 V curve 1, curve 2, curve 3, curve 4 and curve 5 respectively at a constant temperature and concentrate on one temperature, for example $T = 408$ K. At this temperature all the traps are much faster than the experimental time constant so that any trap portion located within the space charge region created by V_{BS} is almost completely ionised. The same discussion applies to other lower temperatures where the traps are partially ionised. The change between curve 1 and curve 5 in

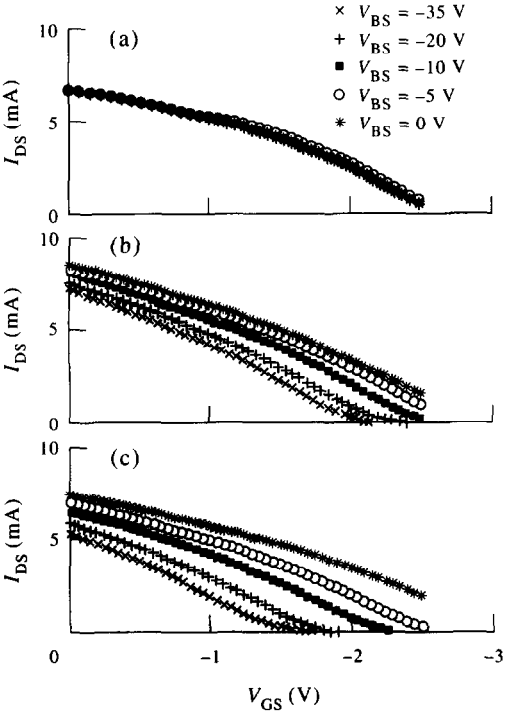

Fig. 5. The $I_{DS}(V_{GS})$ characteristics at different temperatures [(a) 127 K, (b) 255 K and (c) 408 K] with V_{BS} as a parameter for the device F2137/10.

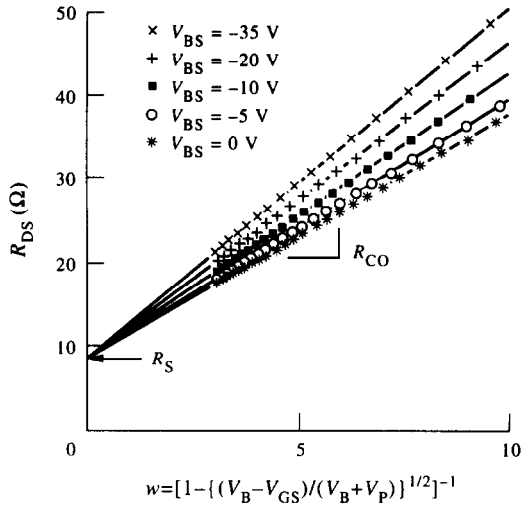

Fig. 6. An example of the transformation of the $I_{DS}(V_{GS})$ characteristics of Fig. 5 to $R_{DS}(w)$ plots (symbols = experimental data; solid lines = fittings) using the best fitted V_P at 408 K with the substrate bias V_{BS} as a parameter.

V_P is $\sim -60\%$, in R_{CO} is $\sim 55\%$ and in R_S is $\sim -10\%$ (Fig. 7). So the changes in V_P and R_{CO} are comparable. This is not expected (theoretically) since if the effect of V_{BS} is to reduce a_0 then it is expected that:

$$\frac{\Delta V_P}{V_P} = -2\frac{V_B + V_P}{V_P}\frac{\Delta R_{CO}}{R_{CO}}. \tag{7}$$

Equation (7) is calculated using:

$$V_B + V_P = \frac{qN_D}{\epsilon_0\epsilon_r}a_0^2 \tag{8}$$

and

$$R_{CO} = \frac{L}{qN_D\mu Z a_0}. \tag{9}$$

For the present device $V_B = 0.75$ V and $V_P \approx 2.85$ V so that (7) becomes:

$$\frac{\Delta V_P}{V_P} \approx -2.5\frac{\Delta R_{CO}}{R_{CO}}. \tag{10}$$

From equation (10), if V_P changes by -60% then (theoretically) R_{CO} would change by 24% only. This is nowhere comparable to the actual experimental result. It was found that this is due to the maximum range of w (w_{max}) used in the fitting[31]. For example when the range of w_{max} changes from 5 to 20, V_P changes by $\sim 2\%$ while R_{CO} changes by $\sim 7\%$. This means that R_{CO} (and hence R_S) are much more sensitive to changes in w_{max} than V_P.

To show that V_P is not significantly affected by this error, the fitting was done for a constant range of a (instead of a constant range of w) up to $a_{min} = 3.7L_D$[31]. At $T = 408$ K the change in V_P was -60%, the change in R_{CO} was $\sim 50\%$. It can be seen that V_P is not affected much while the change in R_{CO} seems to be reduced from the value found previously but not to the expected value of $\sim 24\%$. Therefore the values of V_P, in any case, can be accepted as not affected by the fitting errors. Therefore the value of V_P can be used to evaluate an approximate value for the net ionised impurity density in the substrate. We assume that the interface is similar to an n–p^- junction and the impurities are uniformly distributed. It was found that these are acceptable assumptions[31]. Following a negative voltage applied to the substrate V_{BS}, it can be shown that:

$$\sqrt{V_B + V_P} = \sqrt{\frac{qN_D}{2\epsilon_0\epsilon_r}}(a_0 - a_b)$$
$$= \sqrt{\frac{qN_D}{2\epsilon_0\epsilon_r}}a_0\left(1 - \sqrt{\left(\frac{V_{BI} - V_{BS}}{V_B + V_{PO}}\right)\frac{N_T^-}{N_D}}\right)$$
$$= \sqrt{V_B + V_{PO}}\left(1 - \sqrt{\left(\frac{V_{BI} - V_{BS}}{V_B + V_{PO}}\right)\frac{N_T^-}{N_D}}\right), \tag{11}$$

where a_b is the depletion region spread in the channel because of V_{BS}, V_{PO} is the pinch off voltage corresponding to $V_{BS} = 0$ V, N_D is the doping density in the channel and N_T^- is the net density of ionised traps in the substrate. Therefore by plotting $\sqrt{V_B + V_P}$ vs $\sqrt{V_{BI} - V_{BS}}$, N_T^-/N_D can be evaluated from the slope of the straight line. This plot, at $T = 408$ K, is shown in Fig. 8. It is an acceptable straight line. It was found that $N_T^-/N_D = 8.5 \times 10^{-3}$. If $N_D \approx 1.4 \times 10^{17}$ cm^{-3}

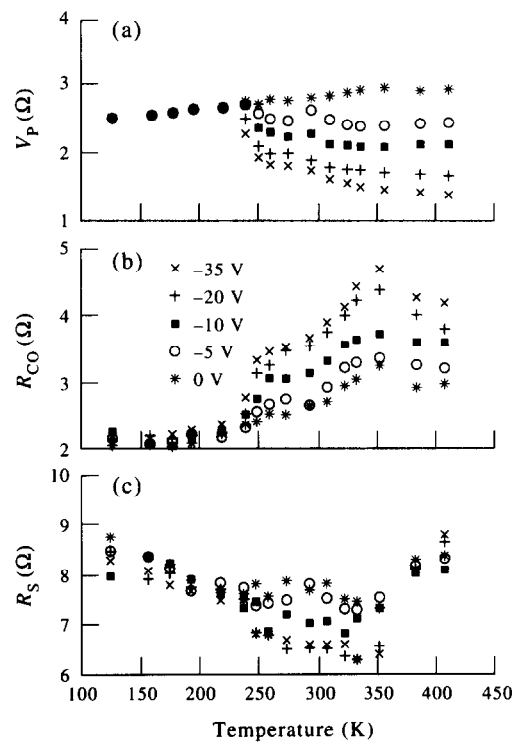

Fig. 7. The device parameters fitting [V_P (a)] or calculated [R_{CO} (b) and R_S (c)] with different substrate biases and their temperature dependence from the fitting in Fig. 6 for the device F2137/10.

(from manufacturer) then $N_T^- \approx N_T \simeq 1.2 \times 10^{15}\,cm^{-3}$. The value for N_T is very acceptable for traps in SI GaAs.

3.3. Substrate conduction

It was found that positive V_{BS} does not have any effect on I_{DS} and I_{BS}[31]. Therefore these results are not presented here. The negative voltage results are shown in Fig. 9. The backgating effect becomes significant above a temperature, which is denoted $T_{th} \sim 240$ K. Below this temperature V_{BS} has a very small effect on I_{DS} and $I_{BS} \propto V_{BS}$.

Before discussing these characteristics in detail some useful information which might be helpful is highlighted. It was found that the temperature dependence of the substrate reverse current at a fixed voltage consists of two regions separated by T_{th}. Below T_{th} the activation energy was evaluated as $\Delta E \leqslant 0.02$ eV. Above this temperature however, the activation energy was evaluated as $\Delta E \approx 0.81$ eV (Fig. 10). It was also found that the evaluated activation energy is independent of the voltage. These observations fit well with the temperature dependence of the non-saturated reverse current observed in silicon, germanium and gallium arsenide real diodes[32]. This temperature dependence of the diode reverse current is usually attributed to the generation component which is proportional to the intrinsic density n_i. Therefore the generation current and the intrinsic density of carriers should have comparable temperature dependence since the active parameters have negligible dependence on temperature as will be shown later. The generation current is usually due to the generation–recombination centres within the space charge region of a reverse biased junction[33]. This is perhaps a first indication that we are dealing with a space charge region at the channel–substrate interface. We will only analyse the densities at temperatures above T_{th} that is when backgating is

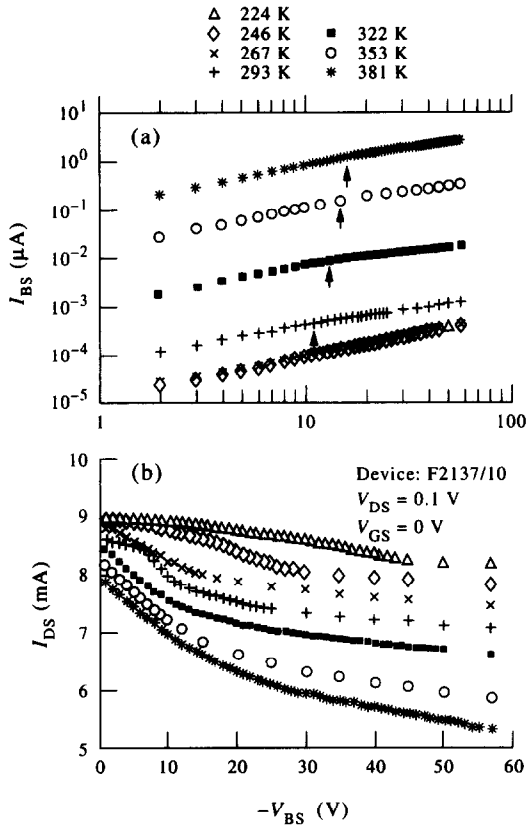

Fig. 9. $I_{BS}(V_{BS})$ and $I_{DS}(V_{BS})$ reverse characteristics at different temperatures. The value of V_I is shown by the arrows in (a).

clearly seen. It is clear that these characteristics show two regions separated at a voltage which will be denoted V_I (absolute value) [Fig. 9(a)]. This voltage increases with increasing temperature. Below V_I the slope of $\log(I_{BS})$ vs $\log|V_{GS}|$ is ~ 0.85. Above V_I this slope is ~ 0.5. The temperature dependence of I_{BS}

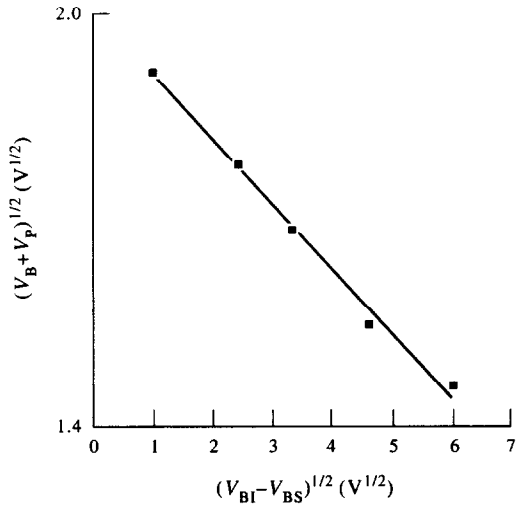

Fig. 8. Evaluation of the ratio N_T^-/N_D at 408 K from the effect of the substrate voltage V_{BS} on the pinch-off voltage V_P. $V_B = V_{BI} = 0.75$ V.

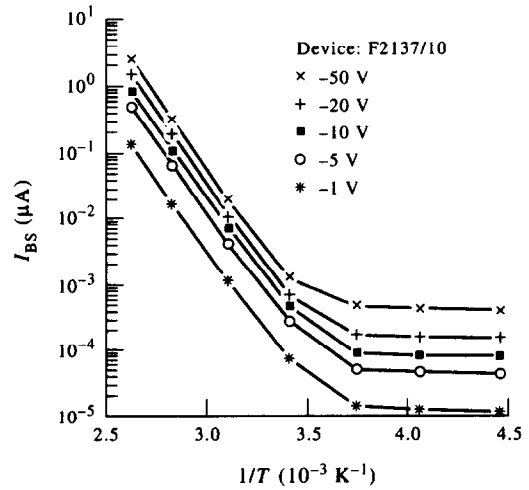

Fig. 10. Temperature dependence of I_{BS} at different fixed voltages.

indicates that it is very likely to be dominated by the generation component which is given by[34]:

$$I_{BS} \approx \frac{qn_i A}{\tau_{eff}} W, \tag{12}$$

where τ_{eff} is the minority carrier effective lifetime in the substrate, A is the cross-sectional area through which the current passes and W is the space charge region width. If the impurities have a uniform distribution, and assuming that the depletion approximation holds and that there is negligible series resistance, then $W \propto \sqrt{V_{BI} - V_{BS}}$ where V_{BS} is the channel–substrate interface built in voltage and therefore it is expected that $I_{BS} \propto \sqrt{V_{BI} - V_{BS}}$. This relation is seen to hold only for $|V_{BS}| > V_1$. However, it is found experimentally that for $|V_{BS}| < V_1$, $I_{BS} \propto |V_{BS}|^{0.85}$. We will now try to explain this behaviour by considering four possible cases[31]. These are:

1. Geometrical effect: the geometrical structure of the mesa implies that the depletion volume and hence the generation current increases with the applied voltage. The angle of the mesa is not sufficient to account for the observed effect.
2. The $I_{BS}(V_{BS})$ characteristics are ohmic with the SI substrate as an ohmic resistance. Its resistance is dependent on V_{BS} due to the spread of the depletion layer width from the interface to decrease the length of the SI substrate resistor. This is an unlikely model since most of the voltage would be dropped across this resistor, rather than the depletion region and hence no backgating should be observed. It was not possible to fit this model to the data making reasonable assumptions.
3. Series resistance: In this case we consider that the current generated from the space charge region (mainly in the buffer layer) passes through a series resistance which is mainly in the SI substrate. We therefore have a current generator and a series resistance which are both voltage dependent. Again this could not be made to fit the observations.
4. Non-uniform profile: In this case the current is entirely dominated by the generation component. The shape of the reverse characteristics is due to the non-uniformity of the impurity distribution (surface or interface like states). This was found to give acceptable results and is detailed below.

In this model we assume that the traps have a certain distribution profile which gives rise to the observed reverse characteristic shape[35]. We also assume that the current is dominated by the generation-component given by eqn (12). Actually we can make use of eqn (12) to evaluate the effective ionised impurities profile in the substrate $N_T(w)$ using the same principle as in the common C–V experiment. In this respect we obtain an expression for $N_T^-(W)$ as:

$$N_T^-(W) \approx -\frac{2\epsilon_0 \epsilon_s q n_i^2 A^2}{\tau_{eff}^2} \frac{\Delta V_{eff}}{\Delta(I_{BS}^2)}, \tag{13}$$

where V_{eff} is the voltage drop in the depletion region. If we assume that there is a series resistance R_{BS} so that:

$$V_{eff} = I_{BS} R_{BS} + V_{BS}, \tag{14}$$

and eqn (13) becomes:

$$N_T^-(W) \approx -\frac{2\epsilon_0 \epsilon_s q n_i^2 A^2}{\tau_{eff}^2} \left(\frac{\Delta V_{BS}}{\Delta(I_{BS}^2)} + \frac{R_{BS}}{2I_{BS}} \right). \tag{15}$$

Taking values of $q = 1.6 \times 10^{-19}$ C, $\epsilon_0 \epsilon_s = 1.14 \times 10^{-12}$ F cm^{-1}, $n_i = 2 \times 10^9$ cm^{-3} at 381 K, $A = 15 \times 10^{-4}$ cm^2 and $\tau_{eff} \sim 10^{-9}$ s the density $N_T^-(W)$ from eqn (15) is plotted as a function of W with R_{BS} as a parameter. W here is calculated from I_{BS} using eqn (12). The results are presented in Fig. 11 in which W_1 is the depletion width corresponding to $|V_{BS}| = V_1$. The purpose of this plot is to find a value for R_{BS} which gives a uniform impurity profile. It seems unlikely that this is possible. If we consider the more probable case where $R_{BS} = 0$ the first observation noticed is the sharp drop of $N_T^-(W)$ right at the beginning of the curve. This may indicate that there exists a fixed charge at the channel–substrate interface[36]. The second observation is that $N_T^-(W)$ becomes very uniform at deeper distances. This observed shape is the same at all temperatures. In order to qualify this model its results are compared with some other experimental results on the same device. It was shown in previous communications[26,27,31] that DLTS, by pulsing the substrate, for the F2137 group shows two hole-like traps (H_1 and H_0). H_1 ($E_A = 0.71$ eV, $T(0.2\text{ s}) = 321$ K) was found to be a bulk trap located in the SI substrate and has approximately a uniform profile while H_0 ($E_A = 0.95$ eV, $T(0.2\text{ s}) = 380$ K) is more likely to be

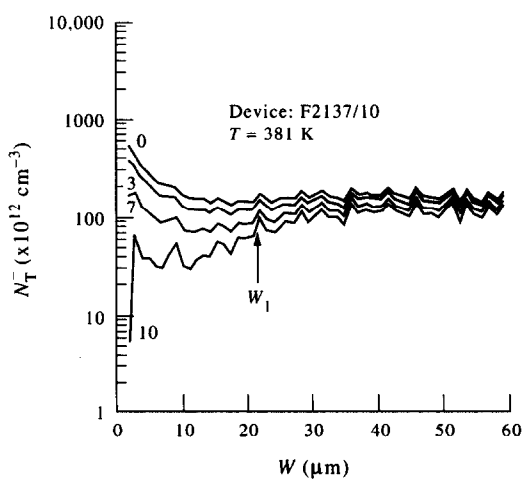

Fig. 11. The approximate impurity profile evaluated from the $I_{BS}(V_{BS})$ characteristics. W_1 is the width corresponding to the voltage V_1 and R_{BS} (MΩ) is the parameter.

an interface trap rather than a real bulk trap. Comparing these results (location of H_1 and H_0) to the profile obtained from the reverse characteristics shows that the fixed charge, which decreases with distance, may be due to the interface trap (H_0) while the uniform profile may be due to the response from the real bulk trap H_1. Finally to qualify this model, we believe that it provides a reasonable and acceptable fit for the results obtained from different experiments. It also confirms the existence of interface states at the channel–buffer interface or more probably at the buffer–substrate interface[36]. The existence of these interface states can explain the observation that the substrate current characteristics change their shape at a voltage V_1. This voltage might be the voltage required for the depletion region to pass through the interface state region. Hence it is the most acceptable one of all models fitted. The depletion width W_1 corresponding to the voltage V_1 is shown in Fig. 11. The absolute value of the W scale is approximate.

4. CONCLUSIONS

The analysis of the backgating effect on the channel conduction of GaAsFETs showed that the main effect of backgating is to reduce the channel width. The reduction of the channel width is the result of ionised hole traps in the substrate side of the channel–substrate interface following a negative voltage applied to the substrate. This relation was obtained by studying the time and temperature dependence of the backgating effect on the device characteristics. The time dependence of the device parameters evaluated by the Fukui fitting procedure is comparable to the time constants of hole-like traps near the channel substrate interface. The temperature dependence of the backgating was related to thermal emission from these hole-like traps. It also confirms the model of a reduction in the channel width. An approximate density of traps was evaluated from the dependence of V_P on V_{BS}. At room temperature the traps responsible for backgating (H_1 and H_0) have time constants of ~ 1 s and ~ 3 min. The effect of EL_2 which has only a small density relative to H_0 and H_1 can be seen in Fig. 7 above 350 K. In other devices we have found that other traps with different characteristics are responsible for backgating at low temperatures (below 150 K).

The relation between backgating and substrate conduction was studied by fitting the reverse $I_{BS}(V_{BS})$ characteristics to several models. It was found that the only model which could explain these characteristics is that there is a space charge region at the channel substrate interface. When this space charge layer is in a reverse bias condition the current is dominated by the generation of electrons and holes from generation–recombination centres in the substrate side of the SCR. The centres might be related to the traps observed by DLTS (H_1, H_0 and EL_2)[26,27,31]. At least two of them (H_1 and EL_2) have activation energies of 0.71 and 0.75 eV respectively, which are close to the intrinsic level and are hence most likely to be active. This model is also able to explain the results from the DLTS and backgating experiments[26,27]. The analysis has indicated that the current is generated in two regions: one is near the channel–substrate interface and the other is in the substrate bulk. In the first region $I_{BS} \propto |V_{BS}|^{0.85}$ which is due to interface states and in the second $I_{BS} \propto |V_{BS}|^{0.5}$ which is due to uniformly distributed bulk traps.

Acknowledgements—We would like to thank Plessey 3-5 for the specimens and discussions. The work benefitted from the collaboration of the other members of the group, M. A. Abdala and Gongjiu Jin. One of us (N.S.) would like to thank the Algerian Government for financial support.

REFERENCES

1. T. Itoh and H. Yanai, *IEEE Trans. Electron Devices* **ED-27,** 1037 (1980).
2. S. Makrem-Ebeid and P. Mimondo, *IEEE GaAs IC Symp.*, pp. 142–144 (1983).
3. P. L. Hower, W. W. Hooper, B. R. Cairns, R. D. Fairman and D. Tremere, *Semiconductors and Semimetals*, Vol. 7, pp. 147–200. Academic Press, New York (1971).
4. C. P. Lee, S. J. Lee and B. M. Welch, *IEEE Electron Device Lett.* **EDL-3,** 97 (1982).
5. C. P. Lee, R. P. Vahrenkamp, S. J. Lee, Y. D. Shen and B. M. Welch, *IEEE GaAs IC Symp.*, pp. 169–172 (1982).
6. P. George, K. Hui, P. K. Ko and C. Hu, *IEEE Trans. Electron Device Lett.* **EDL-11,** 434 (1990).
7. T. Itoh and H. Yanai, *Inst. Phys. Conf. Ser.* **45,** 326 (1979).
8. V. A. Gergel, E. A. Ilichev, A. I. Lukyanchenko, E. A. Poltoratskü and K. S. Shchamkhalov, *Sov. Phys. Semicond.* **26,** 445 (1992).
9. W. S. Lee, *Electron. Lett.* **23,** 587 (1987).
10. W. S. Lee, *Inst. Phys. Conf. Ser.* **91,** 773 (1988).
11. S. Makrem-Ebeid and P. Mimondo, *IEEE Trans. Electron Devices* **ED-32,** 632 (1985).
12. G. J. Papaioannou, J. Kaliakatsos, J. R. Forrest and P. C. Euthymiou, *Inst. Phys. Conf. Ser.* **91,** 733 (1988).
13. S. T. Fu and M. B. Das, *IEEE Trans. Electron Devices* **ED-34,** 1245 (1987).
14. M. A. Abdala and B. K. Jones, *Solid-St. Electron.* **35,** 1713 (1992).
15. M. A. Abdala and B. K. Jones, *Solid-St. Electron.* **36,** 237 (1993).
16. T. Itoh, K. Ohata and F. Hasegawa, *IEEE Trans. Electron Devices* **ED-28,** 876 (1981).
17. W. B. Leigh, J. S. Blakemore and R. Y. Koyama, *IEEE Trans. Electron Devices* **ED-32,** 1835 (1985).
18. T. Nozaki, M. Ogawa, H. Terao and H. Watanabe, *Inst. Phys. Conf. Ser.* **24,** 46 (1975).
19. N. Yokoyama, A. Shibatomi, S. Ohkawa, M. Fukuta and H. Ishikawa, *Inst. Phys. Conf. Ser.* **33b,** 201 (1977).
20. T. Itoh and H. Yanai, *Proc. 11th Int. Conf. Sol. State Dev.*, Tokyo, pp. 351–355 (1979).
21. D. C. D'avanzo, *IEEE Trans. Electron Devices* **ED-29,** 1992 (1982).
22. W. M. Paulson, N. S. Birrittela, T. H. Miers and K. L. McLaughlin, *IEEE GaAs IC Symp.*, pp. 166–167 (1982).
23. K. Yamasaki, N. Kato and M. Hirayama, *IEEE Trans. Electron Devices* **ED-32,** 2420 (1985).

24. C. L. Chen, F. W. Smith, A. R. Calawa, L. J. Mahoney and M. J. Manfra, *IEEE Trans. Electron Devices* **ED-36,** 1546 (1989).
25. M. R. Melloch, D. C. Miller and B. Das, *Appl. Phys. Lett.* **54,** 943 (1989).
26. N. Sengouga and B. K. Jones, *Solid-St. Electron.* **36,** 229 (1993).
27. N. Sengouga and B. K. Jones, *IEEE Trans.* **ED40,** 471 (1993).
28. G. Jin and B. K. Jones, *Semicond. Sci. Technol.* **5,** 395 (1990).
29. G. Jin, Ph.D. thesis, Lancaster University (1991).
30. H. Fukui, *Bell Syst. Tech. J.* **58,** 771 (1979).
31. N. Sengouga, Ph.D. thesis, Lancaster University (1991).
32. A. S. Grove, *Physics and Technology of Semiconductor Devices*. Wiley, New York (1967).
33. C. T. Sah, R. N. Noyce and W. Shockley, *Proc. IRE* **45,** 1228 (1957).
34. S. M. Sze, *Physics of Semiconductor Devices*, 2nd Edn. Wiley, New York (1981).
35. T. Egawa, S. Nozaki, N. Noto, T. Soga, T. Jimbo and M. Umeno, *J. appl. Phys.* **67,** 6908 (1990).
36. D. C. Look, K. R. Evans and C. E. Stutz, *IEEE Trans. Electron Devices* **ED-38,** 1280 (1991).